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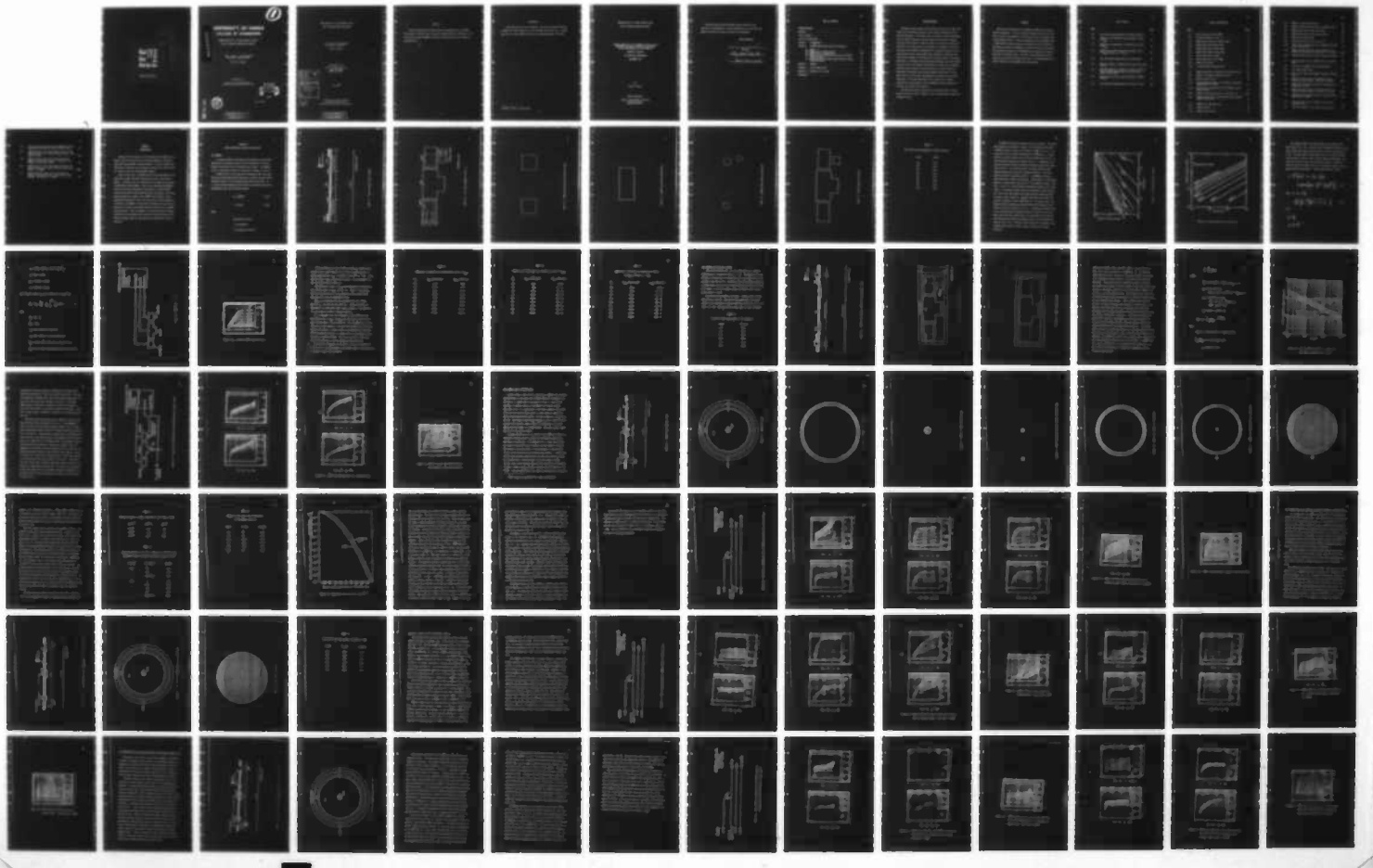

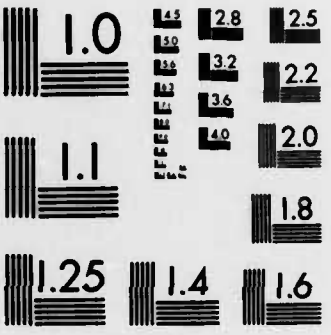

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FABRICATION OF A SILICON MOSFET DEVICE WITH A BIPOLAR TRANSISTOR SOURCE

PROF. JAMES W. HOLM-KENNEDY
PRINCIPAL INVESTIGATOR

DAVID N. OKADA

Sponsored by

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July 1980

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Abstract

A series of MOS devices evolving the direct integration of a Si MOSFET and a bipolar transistor into a single four terminal device is described. The final device, termed an MOSBJT is shown to exhibit gain and novel electronic characteristics.

Introduction

A novel MOS device has been invented.* The device integrates directly an MOSFET and a BJT resulting in a four terminal device with gain. The MOS gate acts as a high impedance control on the operating region of the BJT.

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*Inventor: James W. Holm-Kennedy

C

FABRICATION OF A SILICON MOSFET DEVICE WITH A BIPOLAR TRANSISTOR SOURCE

A THESIS SUBMITTED TO THE GRADUATE DIVISION OF THE UNIVERSITY OF HAWAII IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

IN ELECTRICAL ENGINEERING

DECEMBER 1979

By

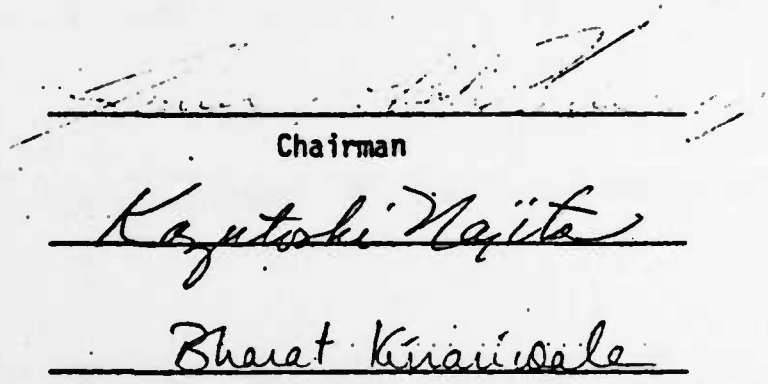
David N. Okada

Thesis Committee:

James W. Holm-Kennedy, Chairman
Bharat Kinariwala
Kazutoshi Najita

We certify that we have read this thesis and that in our opinion it is satisfactory in scope and quality as a thesis for the degree of Master of Science in Electrical Engineering.

THESIS COMMITTEE



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ACKNOWLEDGEMENT

The basic design concept of the devices and the novel ideas incorporated in the devices described in this thesis originated with Dr. James Holm-Kennedy. The author wishes to thank Dr. James Holm-Kennedy for his support, guidance, and many useful clarifying discussions. The author also wishes to thank Paul Saka for his useful discussions and help in the fabrication of the devices, the technical staff consisting of John Johnston, Kamesuke Oshiro, and Melvin Cobb for their conscientious effort toward maintaining, modifying, designing, and fabricating equipment in the University of Hawaii Physical Electronics Laboratory, to Sinthavone Soutavong, Karen Watanabe, and Darrel Motoda for their work in the design and fabrication of the first successful bipolar junction transistor at the University of Hawaii Physical Electronics Laboratory, and to Darrel Motoda and Brian Doi for all their effort in the initial development of the Physical Electronics Laboratory. The author would also like to express his sincere appreciation to Lynn Okumura and Jan Yamamoto for their guidance in preparing and typing the manuscript.

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ABSTRACT

Devices were fabricated that integrated a MOSFET with a bipolar junction transistor. In this new device, minority carriers are injected from the silicon substrate into the base and are collected by the inverted MOSFET channel. Initial investigations were performed using a simple MOSFET structure which was redesigned into a more effective and complex structure (the MOSBJT) to optimize the device performance. The fabrication procedure of the MOSBJT was then modified to improve the bipolar transistor action. The final device performed satisfactorily with a positive transistor gain (β) of ~ 3 and substantial controlled injection into the MOSFET inversion channel.

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CHAPTER 1

INTRODUCTION

The goal of this project was the integration of a MOSFET with a bipolar junction transistor and to provide substantial controlled injection into the MOSFET inversion channel. This was accomplished with several different device structures and basically involves bipolar injection into the inverted MOSFET channel.

Prior to this effort, no MOSFET had ever been fabricated at the University of Hawaii Physical Electronics Lab (or in the State of Hawaii). Therefore, the first objective was to design and fabricate a conventional silicon MOSFET. After it was confirmed that MOSFETs could be sucessfully fabricated in the UH lab, the simple MOSFET structure was modified with additional masks and changes in the fabrication procedure to produce a novel MOSFET with a bipolar source. Acceptable performance of these devices justified the development of a new device, the MOSBJT, in which major considerations were given to achieving a net gain and confining current injection into the MOSFET inverted channel. The first MOSBJT (a diffused structure) performed satisfactorily and attempts were then made to achieve device gain by using an epitaxial layer for the base and an etched mesa region for isolation.

CHAPTER 2

DEVICE FABRICATION, RESULTS AND ANALYSIS

2.1 MOSFET

A n-channel MOSFET was designed and fabricated to confirm that MOS devices of acceptable quality could be fabricated in the new Physical Electronics Lab at the University of Hawaii. This MOSFET was of a conventional design as illustrated in Figures 1.1 and 1.2.

A (100) p-type silicon substrate of thickness 0.014" was used. Four point probe measurements were taken at several locations across the wafer (Table 1.1) to characterize the wafer resistivity. A $\sim$ 1.9 Ω-cm average substrate resistivity was calculated from the V/I measurements using the following equations:

$$\rho_s' = \frac{\ln 2}{\pi} \frac{V}{I} \qquad (1.1)$$

$$\rho = \rho_s'(d) \qquad (1.2)$$

where

ρ_s' ≡ sheet resistance

ρ ≡ resistivity

d ≡ substrate thickness .

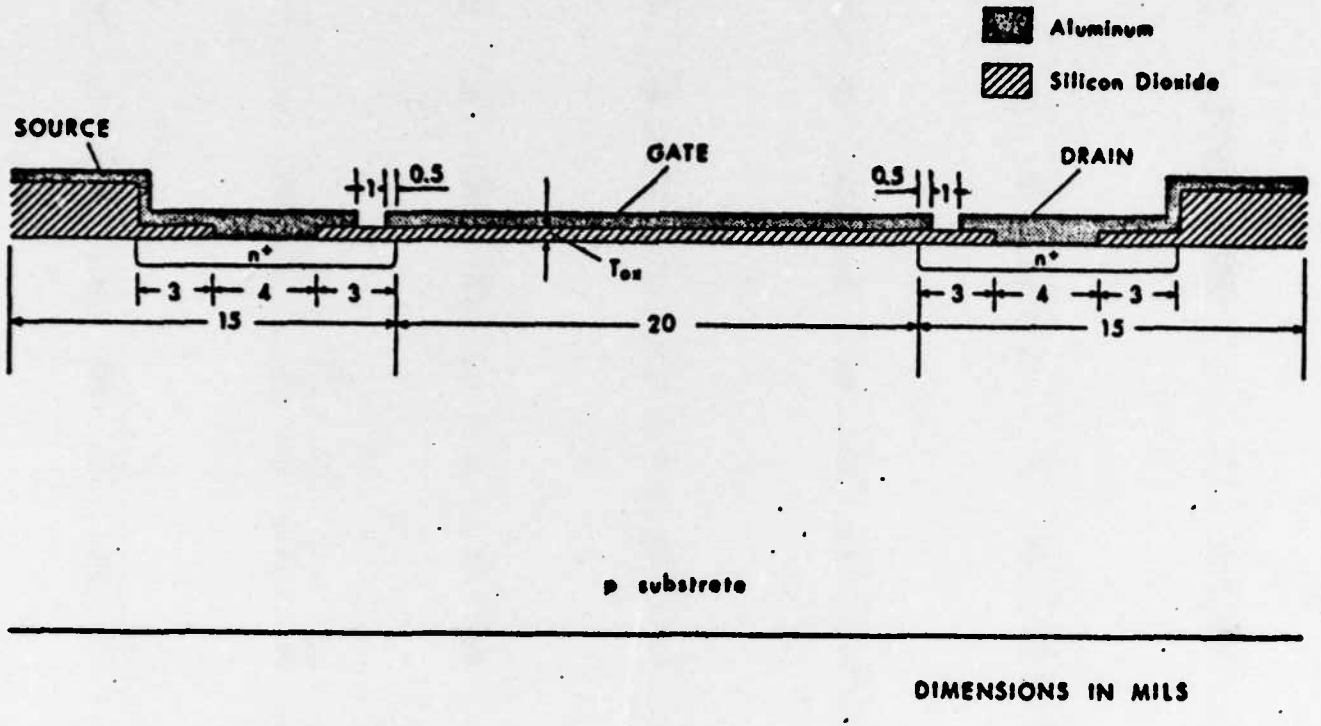

Figure 1.1. Cross sectional view of MOSFET.

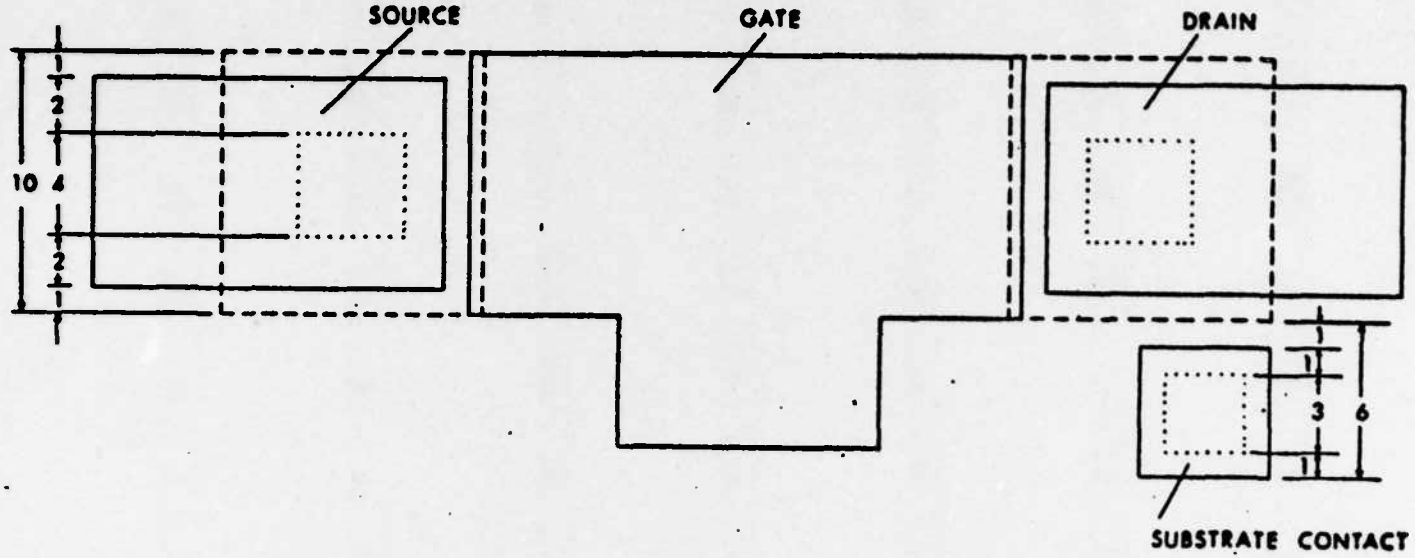

Figure 1.2. Top view of MOSFET of Fig. 1.1.

Figure 1.3. MOSFET source and drain diffusion mask.

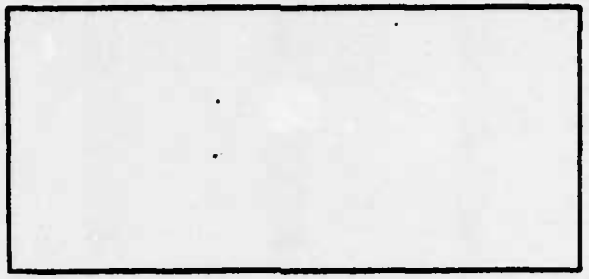

Figure 1.4. MOSFET gate oxide regrowth mask.

Figure 1.5. MOSFET metallization window mask.

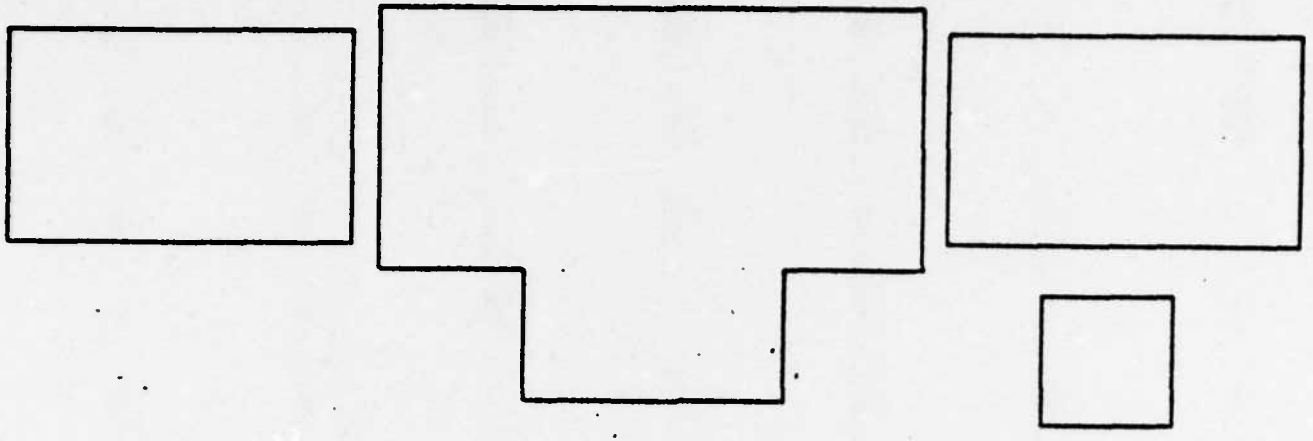

Figure 1.6. MOSFET metallization mask.

TABLE 1.1

Four Point Probe Measurements of MOSFET Substrate

I(μA)	V/I(Ω)
60	12.0
60	12.3
60	12.3
60	11.5
60	11.9
60	12.0
60	11.9
60	12.3

The MOSFET fabrication procedure used was as follows: The wafers were cleaned using procedure 1 (App. A) and a blocking oxide layer of $\sim 5000\text{Å}$ was grown in steam for 80 minutes at 1000C (Fig. 1.7). The oxide color was red violet corresponding to 4600Å (App. B). Source and drain diffusion windows were cut using the mask shown in Fig. 1.3 and the negative photoresist procedure (App. A). A phosphorous predep was performed at 950C (15 minutes) followed by P_2O_5 glass removal with dillute HF. The blocking oxide in the gate region was then removed employing the gate oxide regrowth mask (Fig. 1.4) using a negative photoresist procedure (App. A). A 1000Å gate oxide was grown (100 minute, 1000C dry oxidation). Oxide growth in a dry oxygen ambient is significantly slower than in a wet oxidation process (see Figs. 1.7 and 1.8) and facilitates reproducible growth of thin oxide layers. A 30 minute nitrogen anneal was performed at 1000C followed by a "fast pull" (the wafers were removed from the furnace rapidly) to reduce surface states [2]. The gate oxide color was violet confirming a thickness of about 1000Å (App. B). The source, drain, and substrate contact windows were etched through the blocking and gate oxides using the mask shown in Fig. 1.5. The wafers were then placed into a vacuum system and aluminum deposited at 8×10^{-7} torr for the gate, source and drain contact pads. The metallization was defined using the positive photoresist procedure (App. A) and the metallization mask (Fig. 1.6). The wafers were sintered for 3 minutes at 510C yielding ohmic contacts to the n^+ source, drain and the p-type substrate.

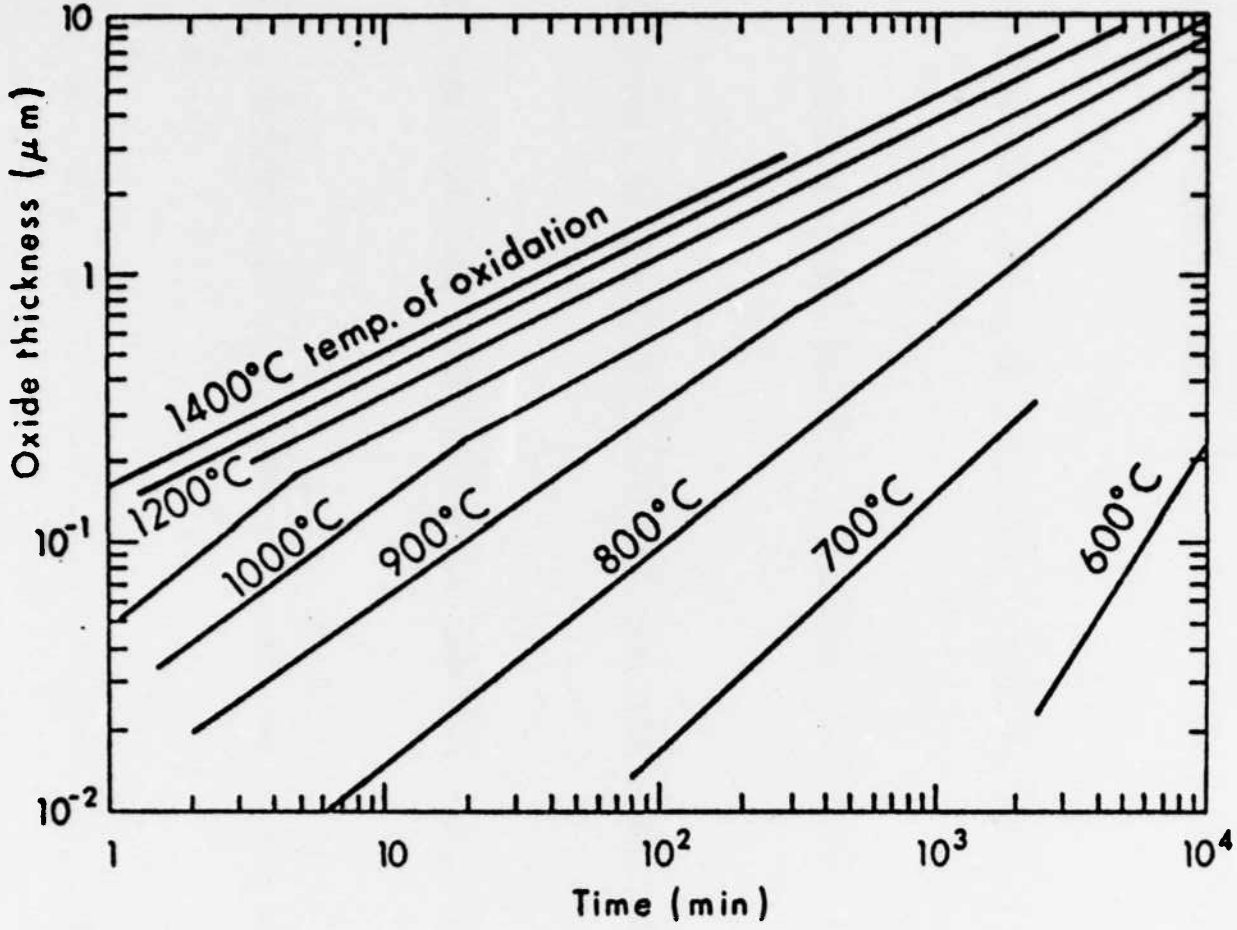

Figure 1.7. Oxide growth rate in steam[1].

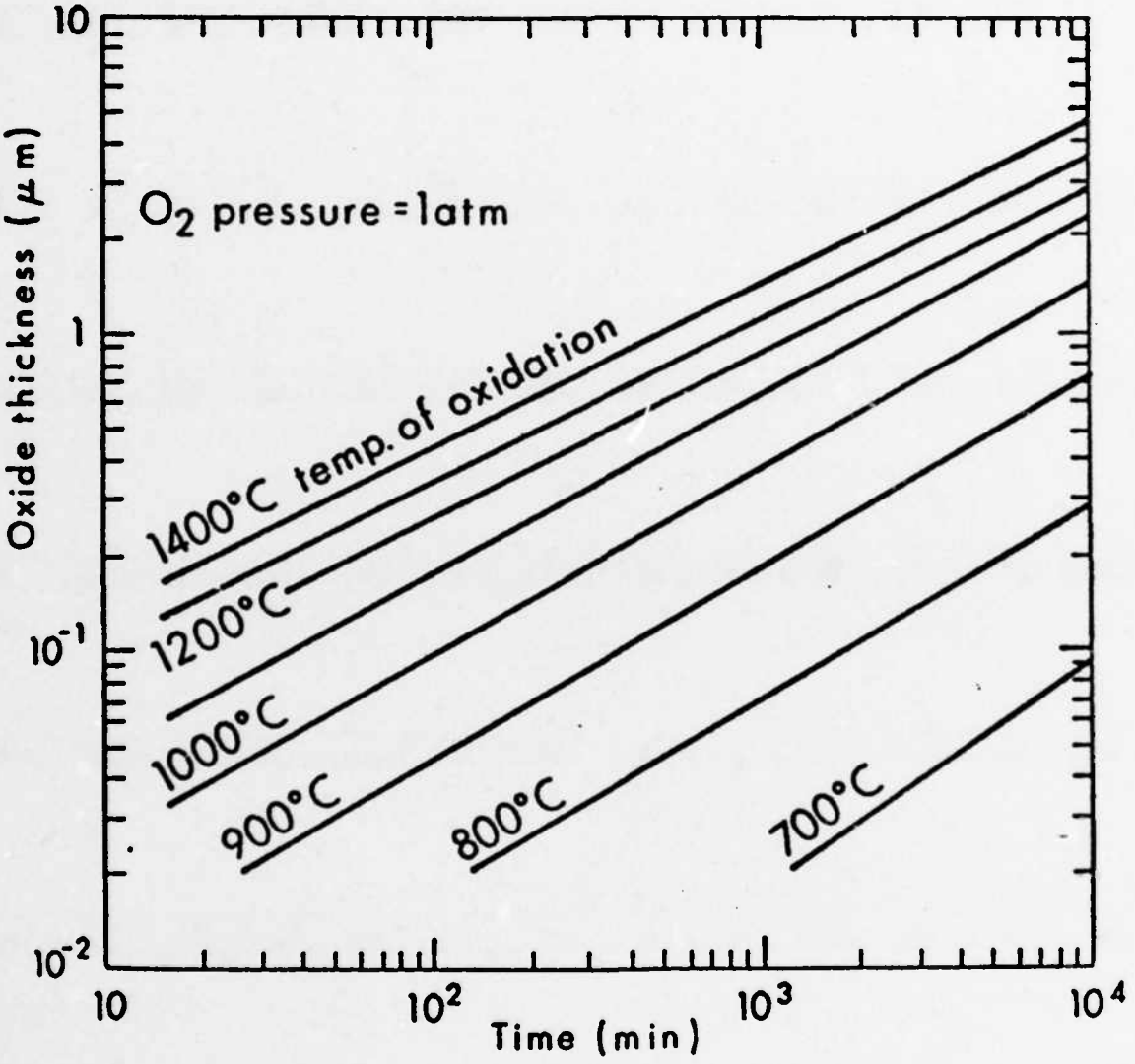

Figure 1.8. Oxide growth rate in dry oxygen[1].

The completed MOSFET was characterized using a Tektronix 576 curve tracer (Fig. 1.9). The curve tracer incremented the gate voltage while measuring the source to drain current versus voltage characteristics. The experimental results shown in Fig. 1.10 can be compared with theoretical source to drain current-voltage relationships. Equations for the drain current and saturation voltage of a MOSFET are derived by Muller and Kamins [6] with a distributed analysis using the gradual-channel approximation. These equations are as follows:

$$I_D = \frac{\mu_n W}{L} \left\{ C_{OX}' \left(V_G - V_{FB} - 2\left|\phi_p\right| - \frac{1}{2}V_D \right) V_D \right.$$

$$\left. - \frac{2}{3}\sqrt{2\epsilon_s qNa} \left[\left(2\left|\phi_p\right| + V_D \right)^{3/2} - \left(2\left|\phi_p\right| \right)^{3/2} \right] \right\} \qquad (1.3)$$

$$V_{DSAT} = V_G - V_{FB} - 2\left|\phi_p\right|$$

$$- \frac{\epsilon_s qNa}{C_{OX}'} \left[\sqrt{1 + \frac{2C_{OX}'}{\epsilon_s qNa}\left(V_G - V_{FB} - V_B \right)} - 1 \right] \qquad (1.4)$$

where

$$C_{OX}' = \frac{\epsilon_{OX}}{X_{OX}}$$

$$\phi_p = \frac{KT}{q} \ln \frac{Na}{n_i}$$

μ_n = Surface mobility $\approx \frac{1}{2}$ bulk mobility.

$V_G \equiv$ Gate voltage.

$V_{FB} \equiv$ Flat-band voltage.

$V_B \equiv$ Substrate voltage.

The flat-band voltage V_{FB} can be expressed as follows [6]:

$$V_{FB} = \Phi_{MS} - \frac{Q_{SS}'}{C_{OX}'} - \frac{1}{C_{OX}'} \int_0^{X_{OX}} \frac{x}{X_{OX}} \rho(x)dx \qquad (1.5)$$

where

$\Phi_{MS} = \Phi_M - \Phi_S$.

$Q_{SS}' = q\, N_{SS}$.

$\Phi_M \equiv$ Work function of the metal.

$\Phi_S \equiv$ Work function of the semiconductor.

$N_{SS} \equiv$ Fixed surface state density per unit area.

$Q_{SS}' \equiv$ Fixed surface state charge density per unit area.

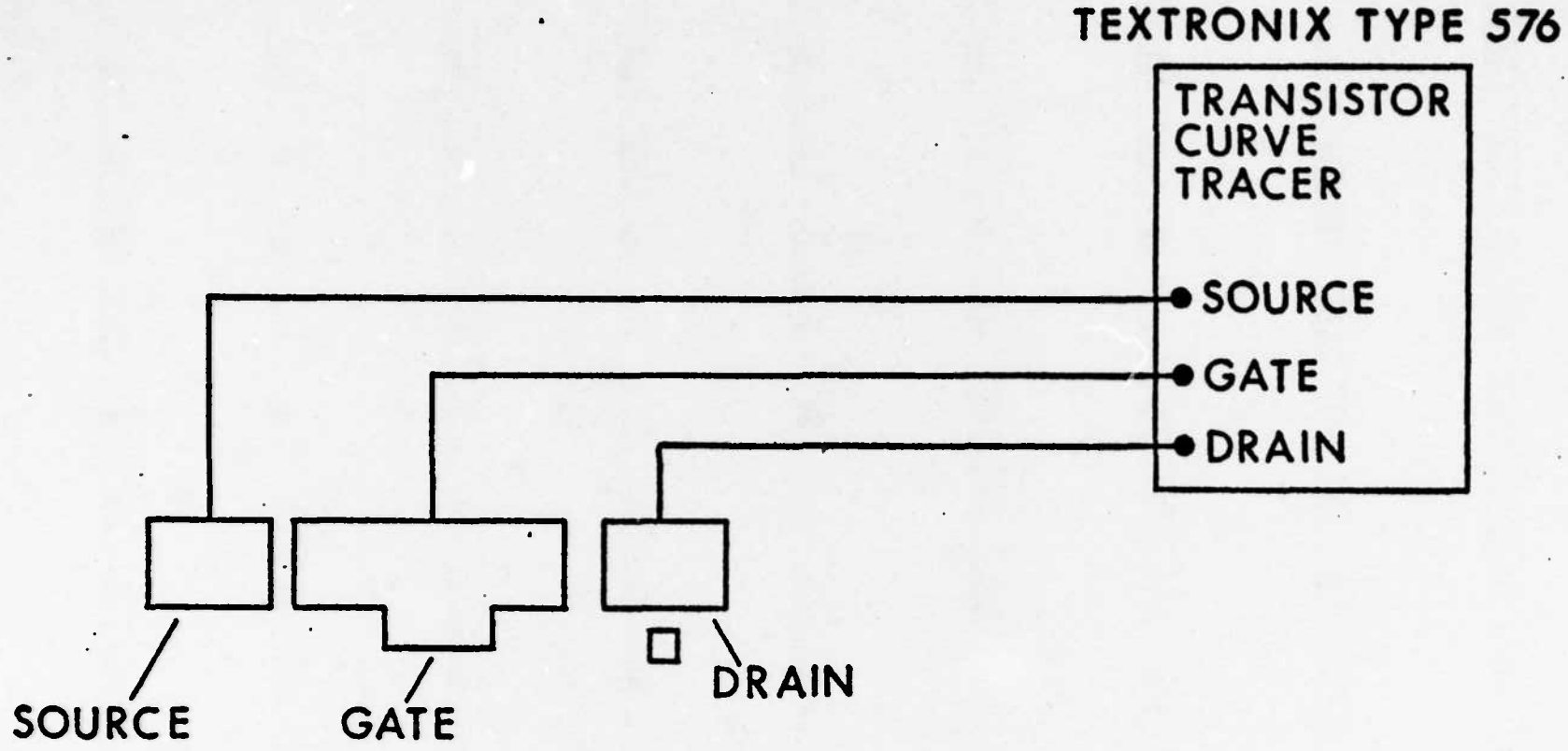

Figure 1.9. MOSFET test circuit.

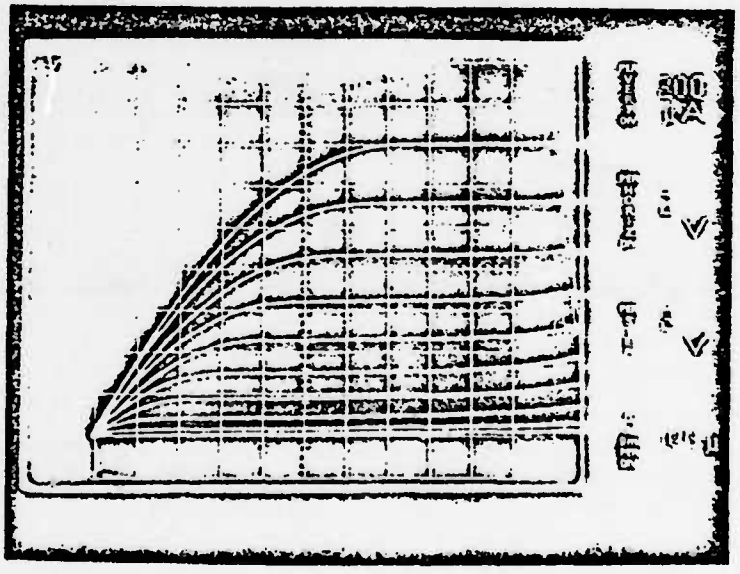

Figure 1.10. n-channel MOSFET characteristics.

In the calculation of the flat-band voltage the integral term resulting from trapped charges in the oxide was neglected and the surface state density, N_{SS}, is assumed to be 8×10^{20} cm $^{-2}$ [2]. Theoretical values of V_{DSAT} calculated using Eq. 1.4 are compared with the experimental data in Table 1.2.

The theoretical values of I_{DSAT} were determined by substituting the computed values of V_{DSAT} into Eq. 1.3. Table 1.3 illustrates that the calculated values of the saturation drain current agree reasonably well with the experimental data.

I_{DSAT} was calculated with the assumption that the surface mobility, μ_n, was half the bulk mobility. A better agreement of experimental and theoretical data, shown in Table 1.4, was obtained if μ_n was taken to be 85% of the bulk mobility.

It is improbable that the difference in the theoretical and experimental data of I_{DSAT} and V_{DSAT} was the result of the surface mobility being 85% of the bulk mobility. The discrepancies are more likely due to the fringing of the gate field increasing the effective width of the channel, a larger surface state density then expected, nonuniform substrate doping, or slight errors in the values of oxide thickness or substrate doping. The latter could not be more accurately confirmed due to lack of appropriate test equipment.

Satisfactory performance of the MOSFET justified proceeding to the next step in the development of the MOSBJT, namely the introduction of a bipolar source into the MOSFET.

TABLE 1.2

Comparison of theoretical and experimental values of V_{DSAT}

V_G	V_{DSAT} Experimental	V_{DSAT} Theoretical
2V	1.5V	0.82V
4V	2.7V	2.1 V
6V	4.3V	3.6 V
8V	6.0V	5.1 V
10V	7.4V	6.6 V
12V	9.2V	8.2 V
14V	11.0V	9.8 V
16V	12.5V	11.5 V
18V	14.5V	13.1 V

TABLE 1.3

Comparison of experimental and theoretical values of I_{DSAT}

V_G	I_{DSAT} Experimental	I_{DSAT} Theoretical
2V	20μA	4.5μA
4V	70μA	29 μA
6V	150μA	76 μA
8V	280μA	148 μA
10V	420μA	247 μA
12V	610μA	371 μA
14V	820μA	524 μA
16V	1070μA	703 μA
18V	1400μA	910 μA

TABLE 1.4

Comparison of calculated and experimental values of I_{DSAT} assuming $\mu_n = .85\mu_B$

V_G	I_{DSAT} Experimental	I_{DSAT} Theoretical
2V	20μA	6.9μA
4V	70μA	45 μA
6V	150μA	117 μA
8V	280μA	227 μA
10V	420μA	380 μA
12V	610μA	570 μA
14V	820μA	806 μA
16V	1070μA	1080 μA
18V	1400μA	1400 μA

2.2 MOSFET with a Bipolar Source

The previous MOSFET (Sec. 2.1) was fabricated in a p region diffused into a n substrate (Figs. 2.1, 2.2). The approach was used because of relative ease of fabrication and to test the initial integration of the BJT and FET. Forward biasing the substrate (emitter)/ p region (base) junction, while reverse biasing the inversion channel with respect to the base region provides the MOSFET with a distributed "bipolar" source.

The fabrication proceeded as follows. A (100) n-type silicon substrate was selected. Four point probe measurements were made (Table 2.1) to determine an average substrate resistivity of 5.1 Ω-cm (Eqs. 1.1, 1.2). The wafers were cleaned (App. A) and a 80 minute

TABLE 2.1

Four point probe measurements of the substrate

I (mA)	V/I (Ω)
1.0	20.1
1.0	23.7
1.0	20.5
1.0	24.6
1.0	21.0
1.0	24.8

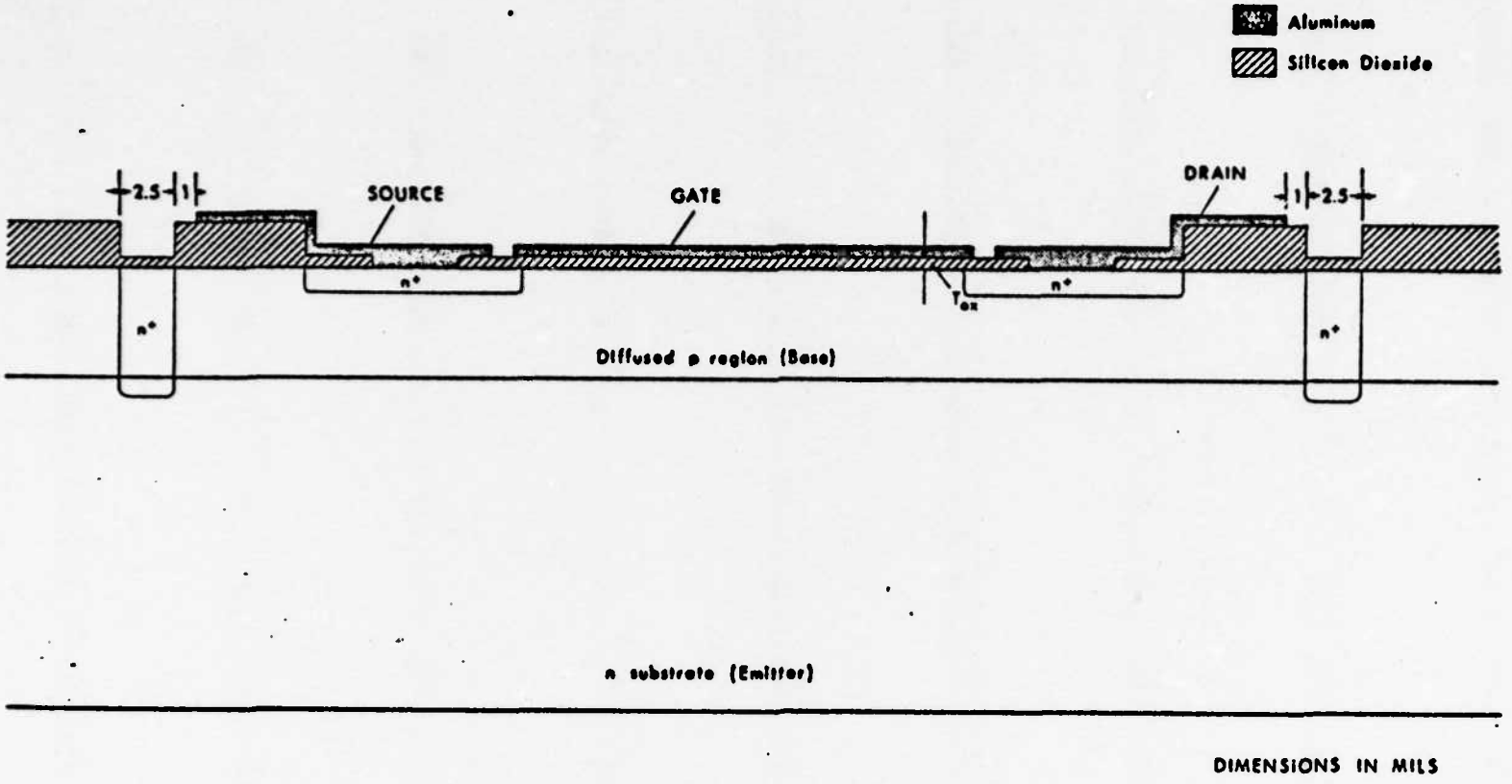

Figure 2.1. MOSFET with bipolar injection cross sectional view.

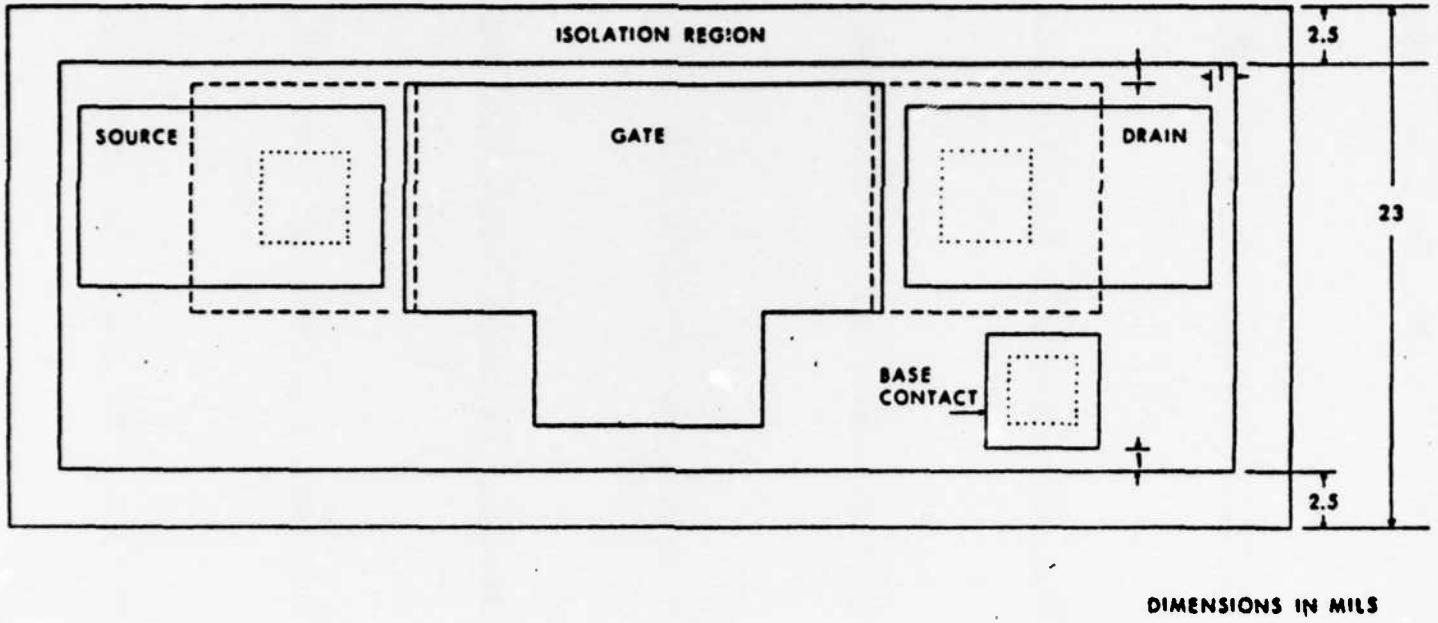

Figure 2.2. MOSFET with bipolar injection top view.

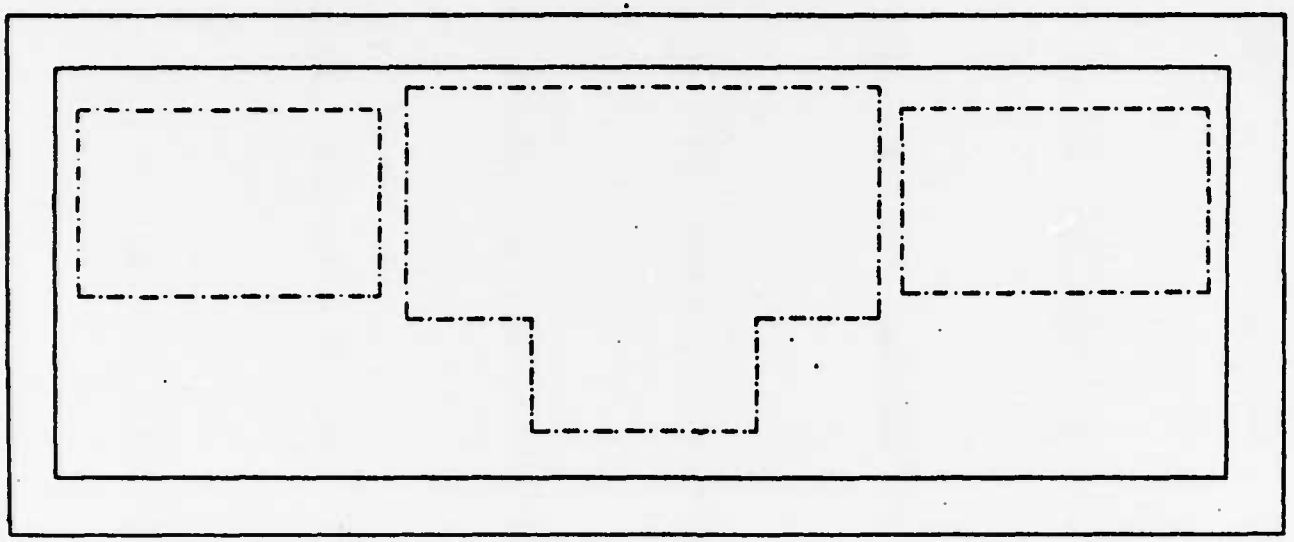

Figure 2.3. MOSFET isolation mask.

1000C wet oxidation process performed (Table 1.2), resulting in a blue violet oxide corresponding to 4800Å (App. B). The blocking oxide layer was left on the back of the wafer to prevent the doping of the substrate contact (the back of the wafer) during the base diffusion. This was achieved by protecting the back of the wafer with negative photoresist during the removal of the oxide on the front surface of the wafer. Operation of the FET/BJT device imposes constraints on the base doping profile. The diffused p-layer must have a sufficiently low surface concentration to allow the inversion layer to form at modest gate voltages. Since a lighter doping profile results in a deeper depletion into the base at inversion (Fig. 2.4), the base width should be of sufficient thickness to prevent the drain/base junction depletion region from extending through the base but should be narrow for a large gain. To achieve the appropriate base profile a 750C 15 minute predep was performed followed by a dillute HF etch to remove the B_2O_3 glass and therefore reduce the surface concentration of the final diffusion profile. The predep layer was driven at 1150°C for 6 hours in a dry oxygen ambient during the first hour and 45 minutes to grow a blocking oxide preventing out diffusion, in nitrogen for 3 hours and 41 minutes, and in steam during the final 34 minutes to increase the oxide thickness to $\sim$ 6000Å (Fig. 1.3). This procedure led to a calculated junction depth of 3.7 μm and a surface concentration of 3.2×10^{16} cm^{-3} determined from the following equations [4]:

$$\frac{Q}{A} = \frac{2N_0}{\sqrt{\pi}} \sqrt{D_B t_B} \qquad (2.1)$$

where

$\frac{Q}{A}$ ≡ Total number of impurity atoms per area.

N_0 ≡ Solid solubility.

Boron at 725C 2.2×10^{20} cm^{-3} (Appendix B).

D_B ≡ Diffusivity of Boron.

725C 10^{-7} μ^2/h (Appendix B)

1100C 1.6×10^{-1} μ^2/h

t_B ≡ Length of predep; and

$$N_A(x,t_d) = \frac{Q}{A} \frac{1}{\sqrt{\pi D_B t_d}} e^{-x^2/4D_B t_d} \qquad (2.2)$$

where

$N_A(x,t_d)$ ≡ Doping profile of impurity atoms.

$\frac{Q}{A} \frac{1}{\sqrt{\pi D_B t_d}}$ ≡ Surface concentration.

t_d ≡ Length of drive.

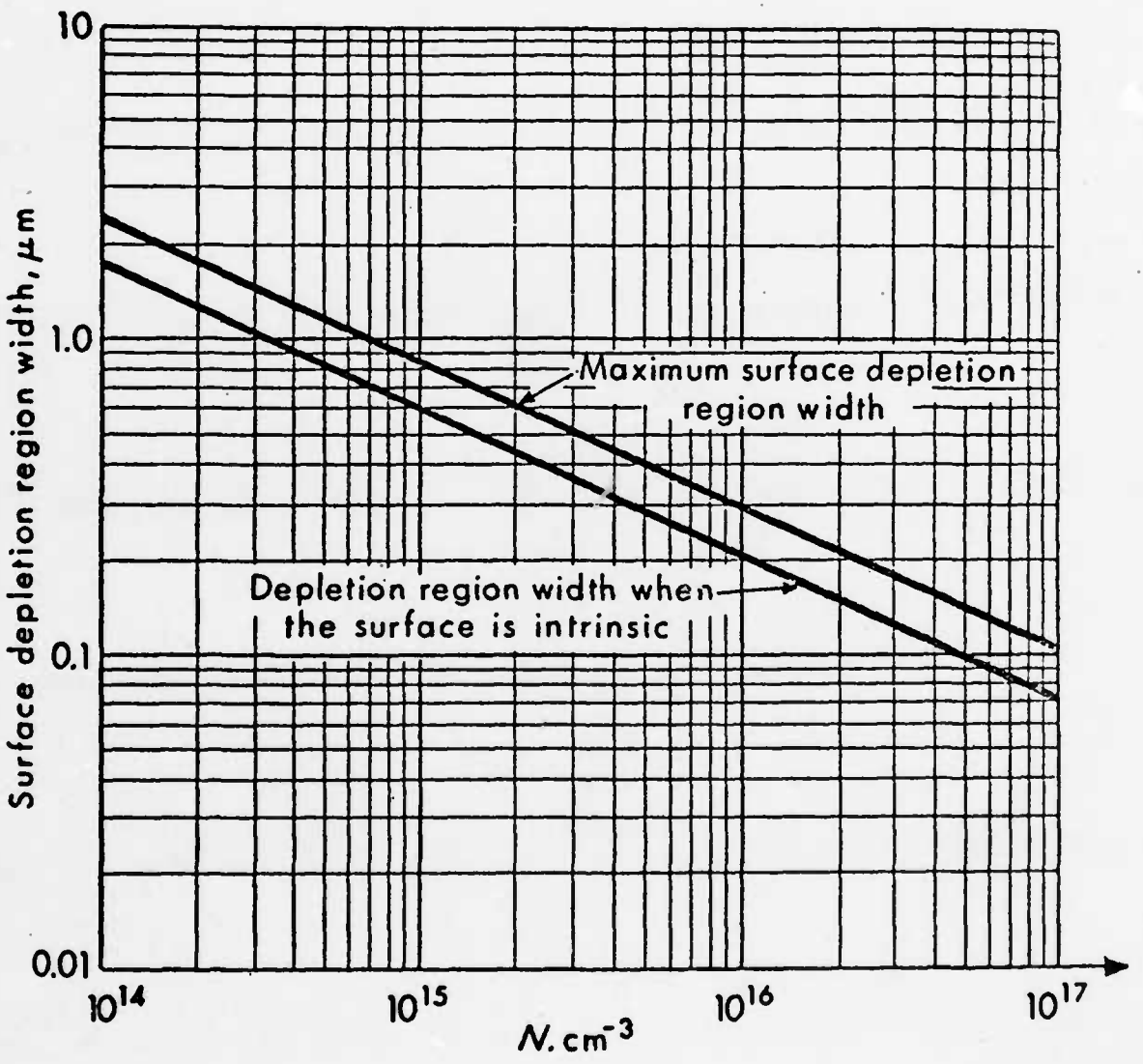

Figure 2.4. Surface depletion width as a function of the doping concentration in silicon.[3]

A phosphorous diffusion designed to compensate the diffused base profile was performed to electrically isolate the devices. The negative photoresist procedure (App. A) and the isolation mask (Fig. 2.3) was used to define and etch a window in the oxide. A 30 minute 1000C predep was performed, followed by a dillute HF etch and a 3 hour drive during which a dry oxide was grown for 20 minutes. Within this isolation region, the MOSFET of Chapter 2.1 was fabricated (see Fig. 2.2).

The devices were characterized using a Tektronix Type 576 curve tracer and the circuit illustrated in Fig. 2.5. The dependence of bipolar transistor characteristics on gate voltage (Fig. 2.6) reveal that increased gate voltage results in increased collector current and gain of the device. Increased gate voltage results in the enhancement of the inversion layer density and as a consequence channel saturation occurs at a larger value of collector current. The observed increase in gain when the gate voltage is increased is probably due to the dependence of the current collecting capability of the inversion layer (without saturation effects) on the inversion layer density. Figure 2.7 displays the "reverse" BJT characteristics, in which the substrate is the collector and the drain contact is the emitter. The substantial gain results from a favorable drain/base junction injection efficiency and a significant collector area. The effect gate voltage had on the BJT characteristics confirmed the successful integration of a BJT and FET and it was then appropriate to proceed to the next level of device design.

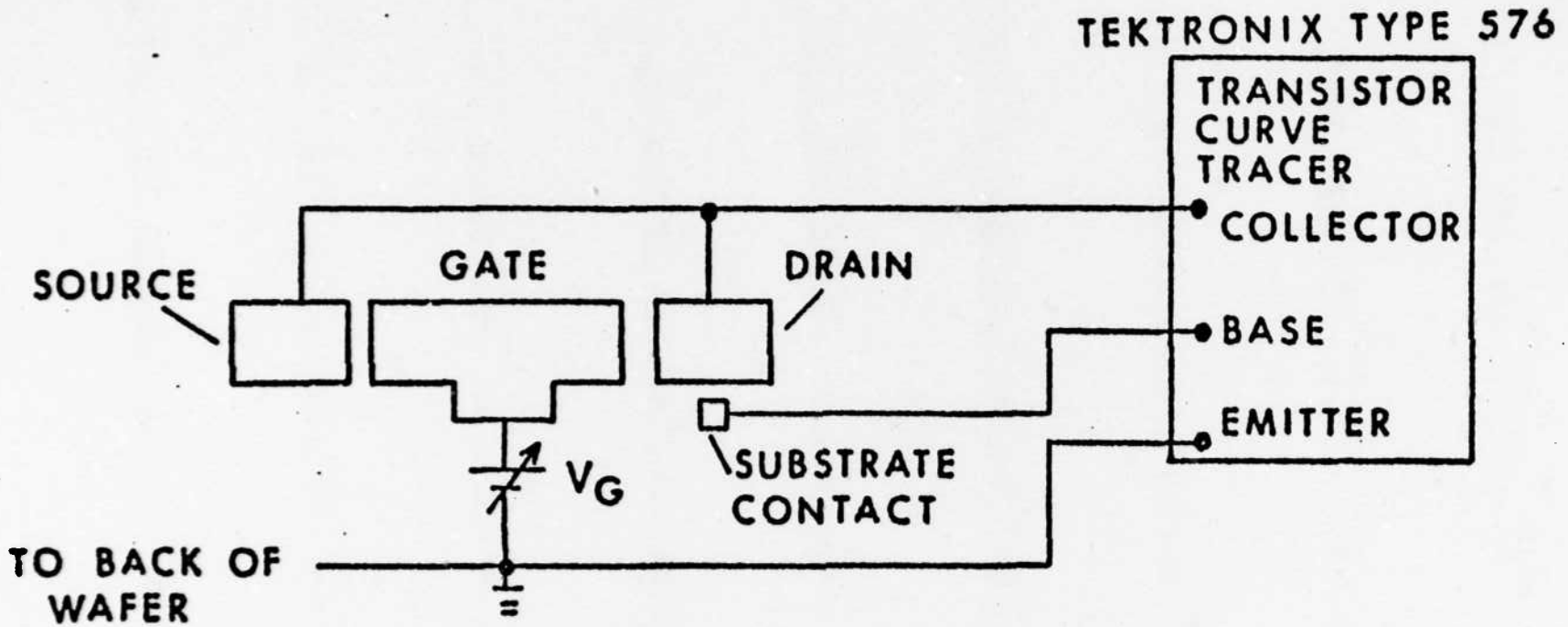

Figure 2.5. Test circuit configuration for the MOSFET having a bipolar source.

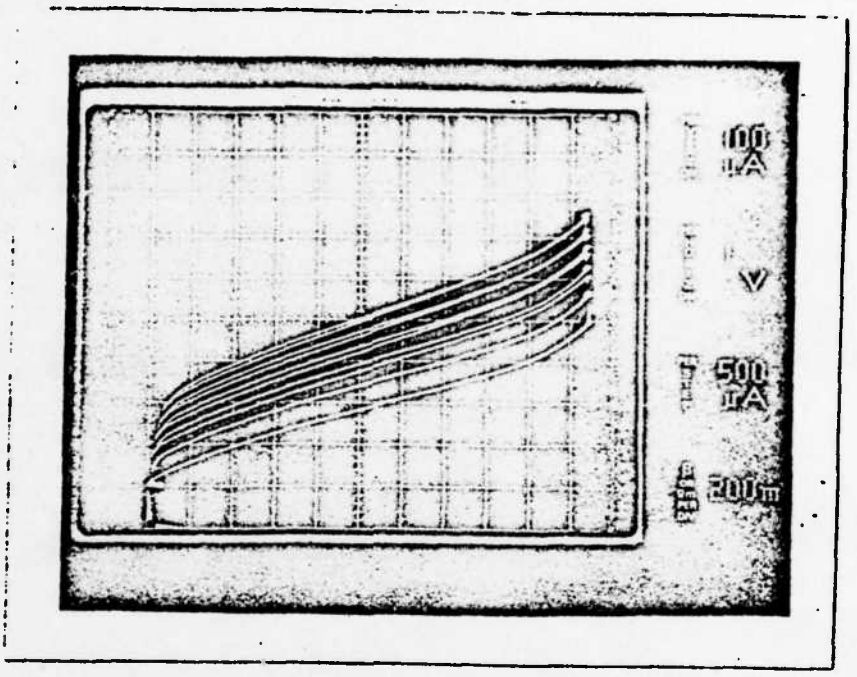

Fig. 2.6a. V_G = 0V

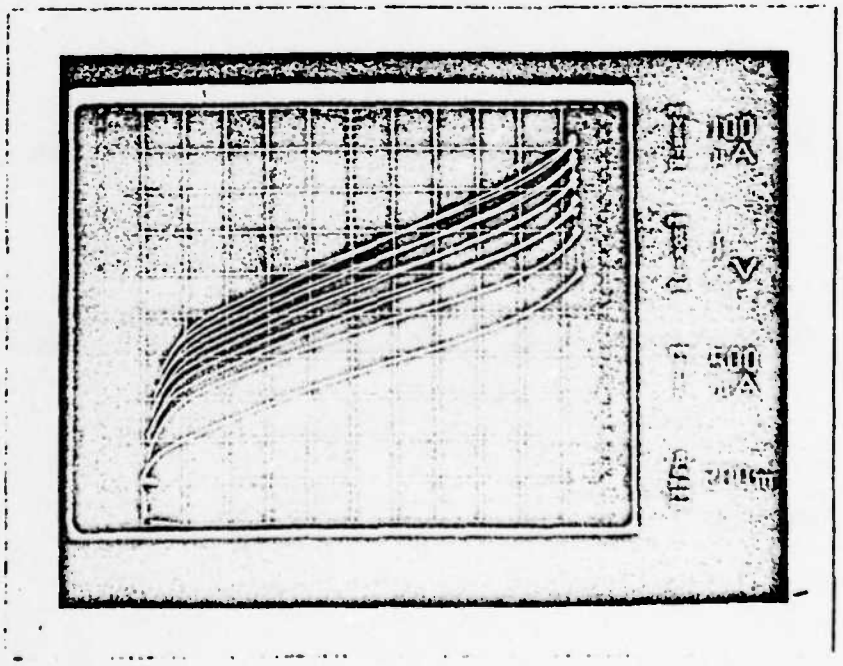

Fig. 2.6b. V_G = 10V

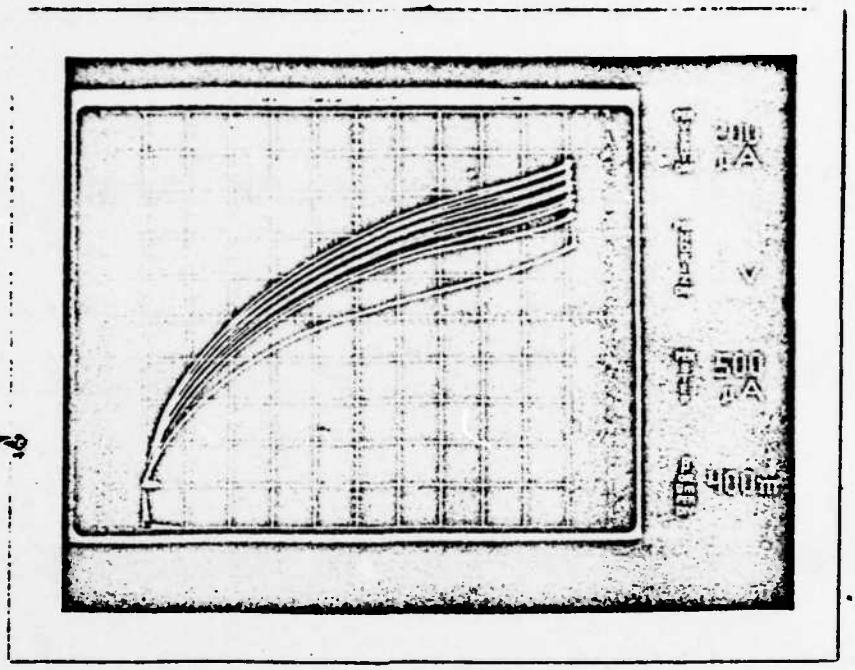

Fig. 2.6c. V_G = 15V

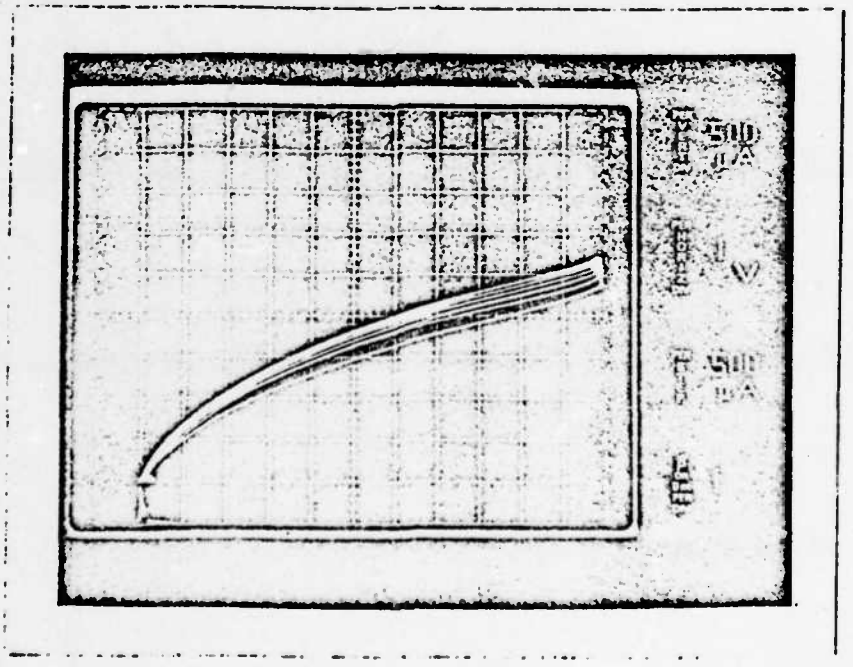

Fig. 2.6d. V_G = 20V

Figure 2.6. MOSFET BJT characteristics as a function of V_G.

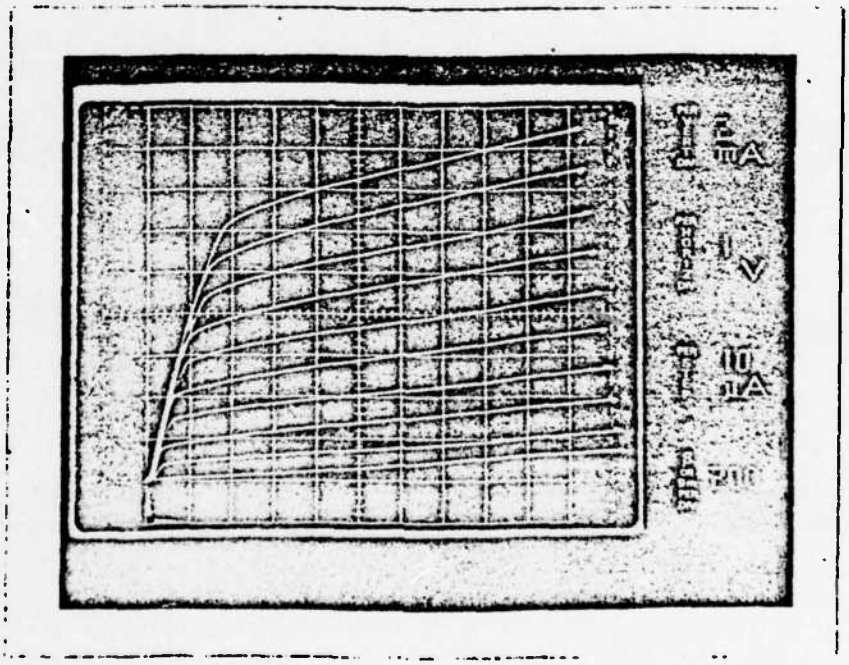

Figure 2.7. MOSFET "reverse" BJT characteristics.
(Drain-Emitter, Substrate-Collector)

2.3 MOSBJT with a Diffused Base

A novel device, which will be called here a MOSBJT, was designed[1] and fabricated in the University of Hawaii Physical Electronics Lab. The device is schematically represented in Figs. 3.1 and 3.2 and operates in a manner similar to the MOSFET with bipolar source described in Sec. 2.2, except that it provides a geometry consistent with the final device target, which is a MOS inversion mode device with a distributed bipolar source. The device operates in the following way: the forward biased substrate/base junction injects minority carriers into the base, some of which is collected by the reverse biased inverted channel of the MOS device. Thus, here the BJT takes the place of the source contact.

A major consideration in the design of the MOSBJT was given to a structure confining the BJT injection to the MOSFET channel while providing a net BJT gain. To accomplish this a large circular gate was chosen to minimize current crowding, provide symmetry, increase the collector area, and assist in the confinement of the injected current to the vicinity of the collector (MOS channel). A large gain requires that the base width be much less than the diffusion length. On the other hand a limiting factor to the base width is punch through, which occurs when the base depletion (resulting from applied voltages) extends through the base. Further, the performance of the MOSBJT is strongly dependent on the impurity concentration in the base

[1] Basic design was provided by Dr. James Holm-Kennedy.

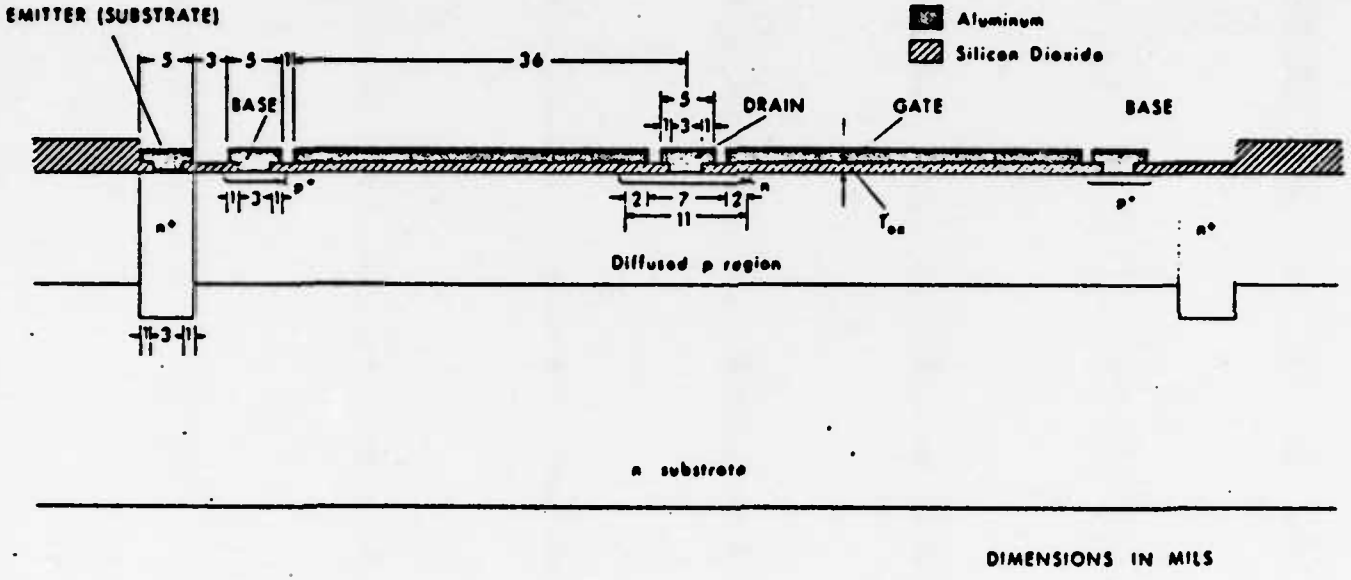

Figure 3.1. MOSBJT cross sectional view.

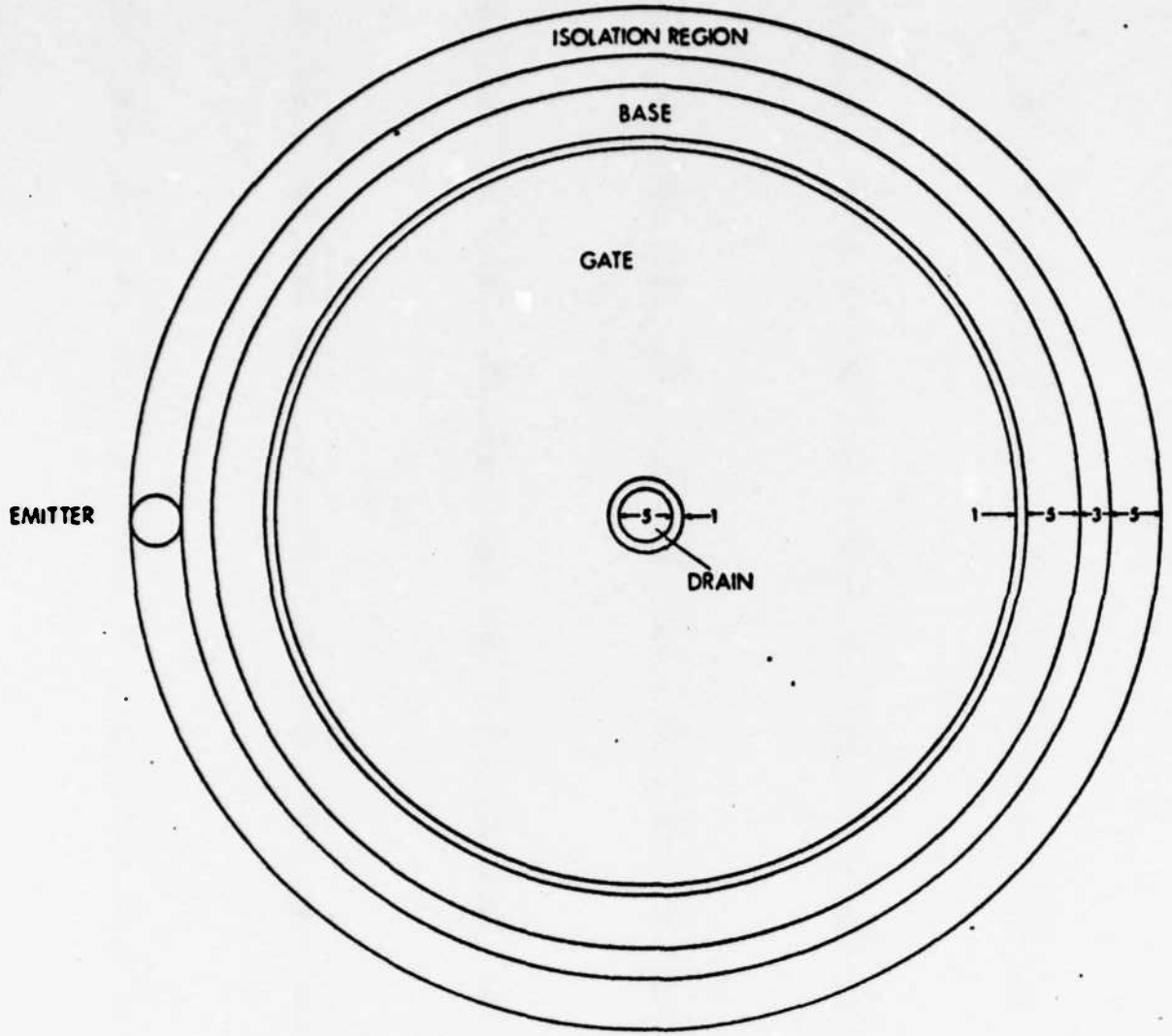

Figure 3.2. MOSBJT top view.

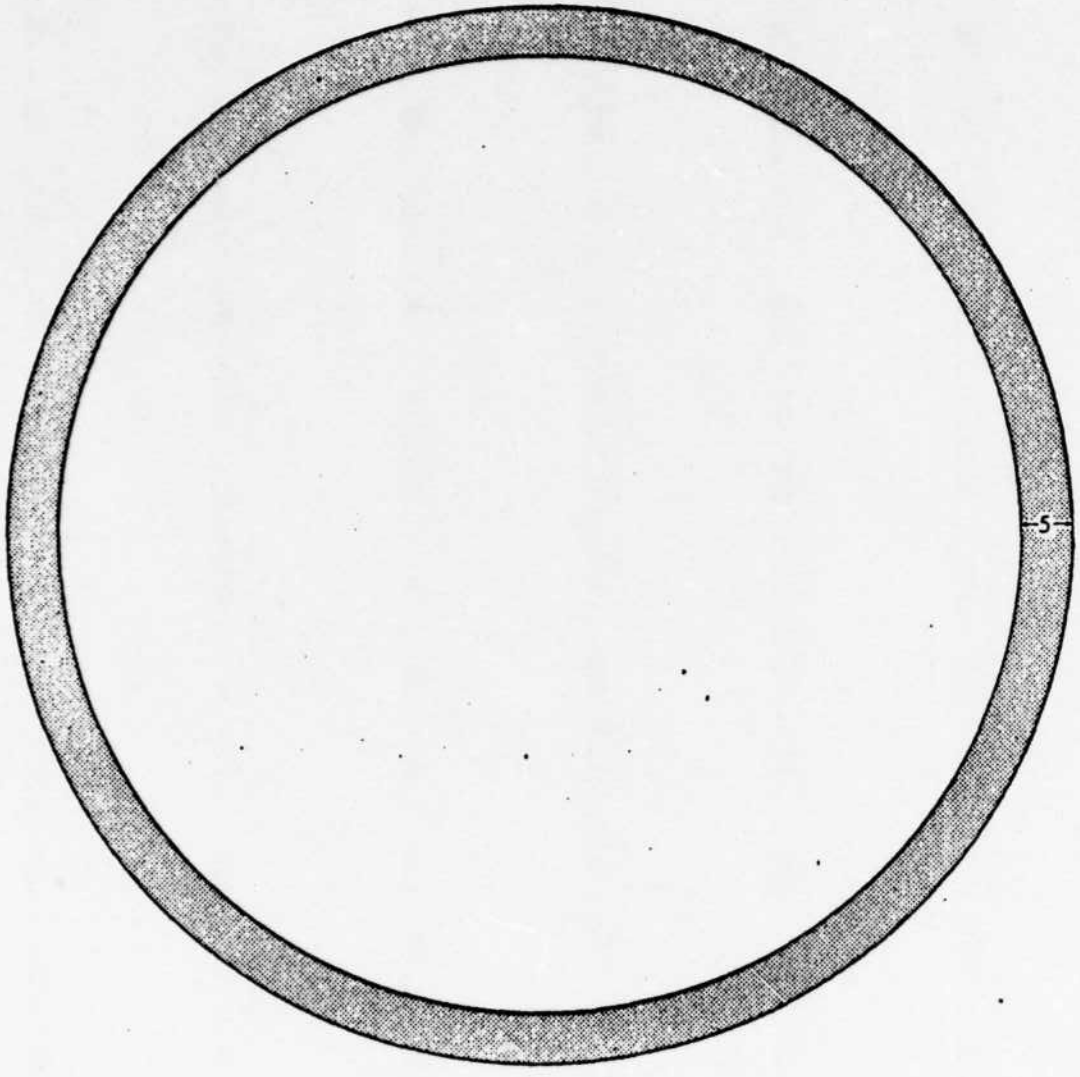

Figure 3.3. MOSBJT isolation mask.

Figure 3.4. MOSBJT n^- drain diffusion mask.

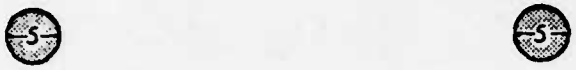

Figure 3.5. MOSBJT substrate and drain contact diffusion mask.

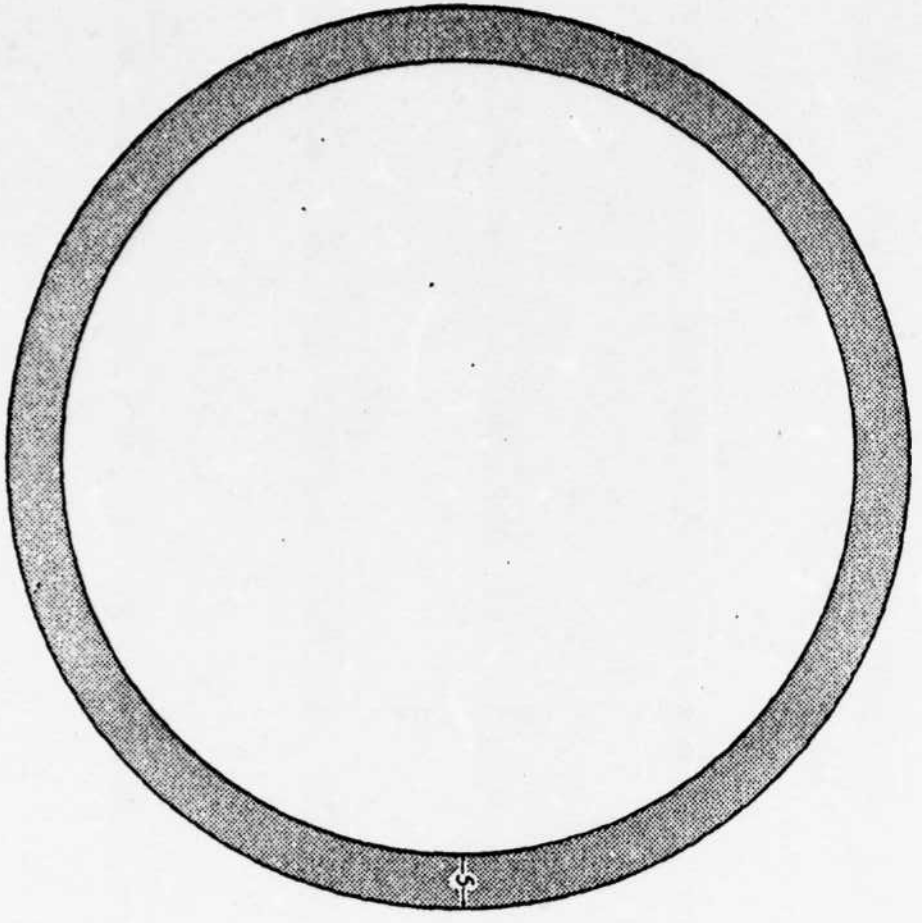

Figure 3.6. MOSBJT base contact and diffusion mask.

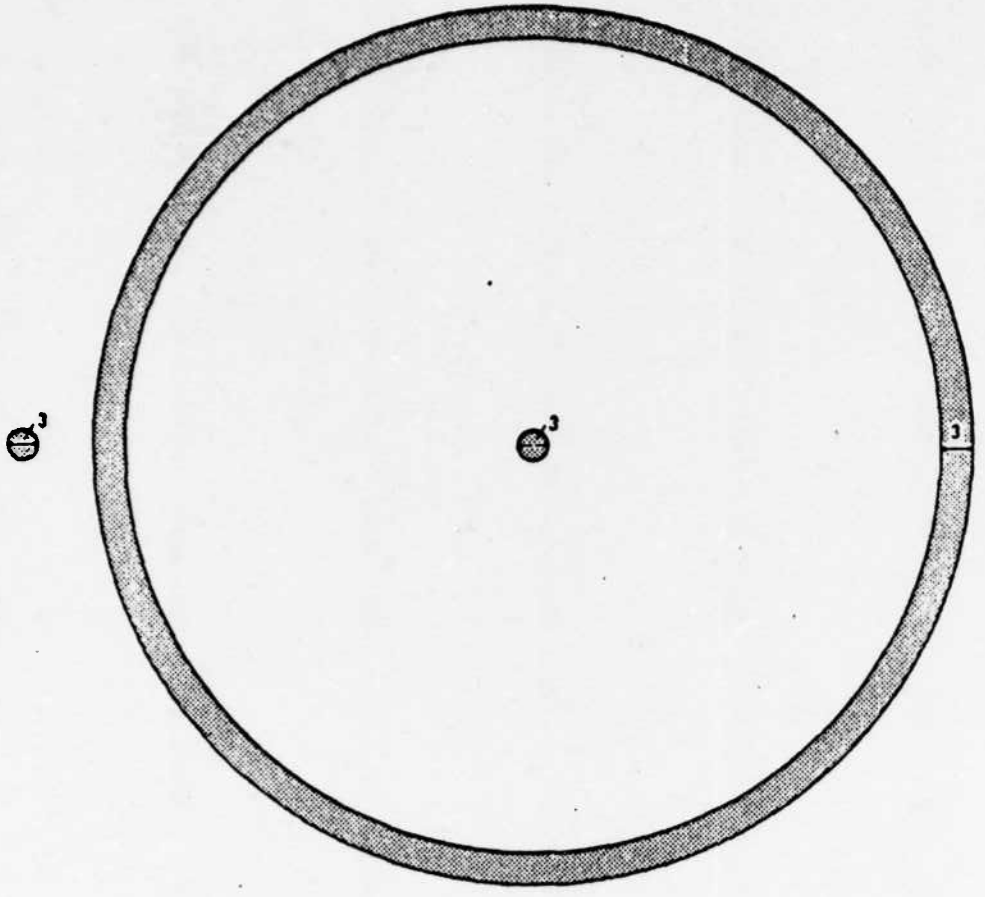

Figure 3.7. MOSBJT metallization contact window mask.

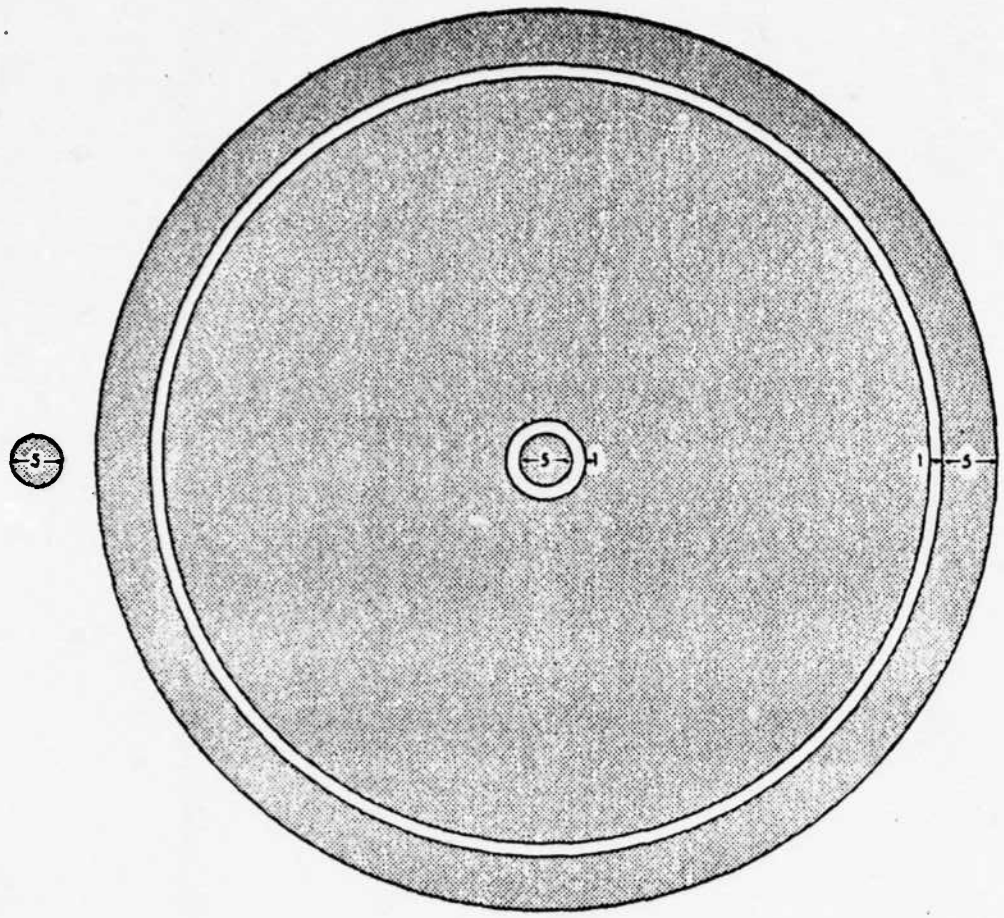

Figure 3.8. MOSBJT metallization mask.

region. For a large gain one desires a lightly doped, narrow base and a long minority carrier diffusion length (Table 3.1). The resistivity of the base region also controls the drain/base breakdown voltage and depletion depth (Table 3.2) as well as the depletion into the base due to V_g (Fig. 2.4).

The device fabrication and processing proceeded as follows. Consistent with the above device design constraints, a (100) 2-4 Ω-cm, 0.013" thick, n-type silicon substrate was chosen. Four point probe measurements (Table 3.3) revealed its resistivity to be ∿ 2.8 Ω-cm (Eqs. 2.4, 2.5). The wafers were cleaned (App. A) and a 750C, 30 minute boron predep performed followed by a dillute HF etch to remove the B_2O_3 glass. The predep was driven in at 1150C for 19 hours in a wet oxygen ambient during the first 45 minutes and in dry nitrogen for the remaining time. The result was a violet oxide ∿ 4600Å (App. B). This procedure led to a calculated surface concentration of 7.6×10^{16} cm^{-3} and a junction depth of 6.9 μm (Eq. 2.1 and 2.2). The negative photoresist procedure (App. A) was used with the isolation mask (Fig. 3.3) to create a circular window in the blocking oxide. The following phosphorous predep yielded a erfc impurity profile. The normalized erfc curve (Fig. 3.9) was used to determine that a 2.7 hour 1100C process would result in an impurity profile that compensates the base impurity profile forming the isolation region and substrate contact.

The drain contact diffusion consisted of two steps. First an initial light phosphorous predep was performed before the gate oxide

TABLE 3.1

Diffusion length vs. doping concentration for p-type silicon[5]

N_A cm^{-3}	ρ(Ω-cm)	L_n(μm)
5×10^{17}	0.1	46
2×10^{16}	1.0	79
1×10^{15}	10.0	155

TABLE 3.2

Depletion depth as a function of doping and reverse bias for homogeneous doped, one-sided abrupt planar diode at 300°K[6]

ρ (Ω-cm)	V_R (Volts)	X_d (μm)
0.1	10	1.0
	20	1.2
	45 (B.D.)	2.0
1.0	1	1.0
	10	3.0
	30	5.0
	90	9.0
	200 (B.D.)	10.6

TABLE 3.3

Results of four point probe measurements of the MOSBJT substrate

I (mA)	V/I (Ω)	ρ (Ω-cm)
1.0	19	2.8
1.0	19	2.8
1.0	19.5	2.9
1.0	19.5	2.9
1.0	19.5	2.9
1.0	19	2.8

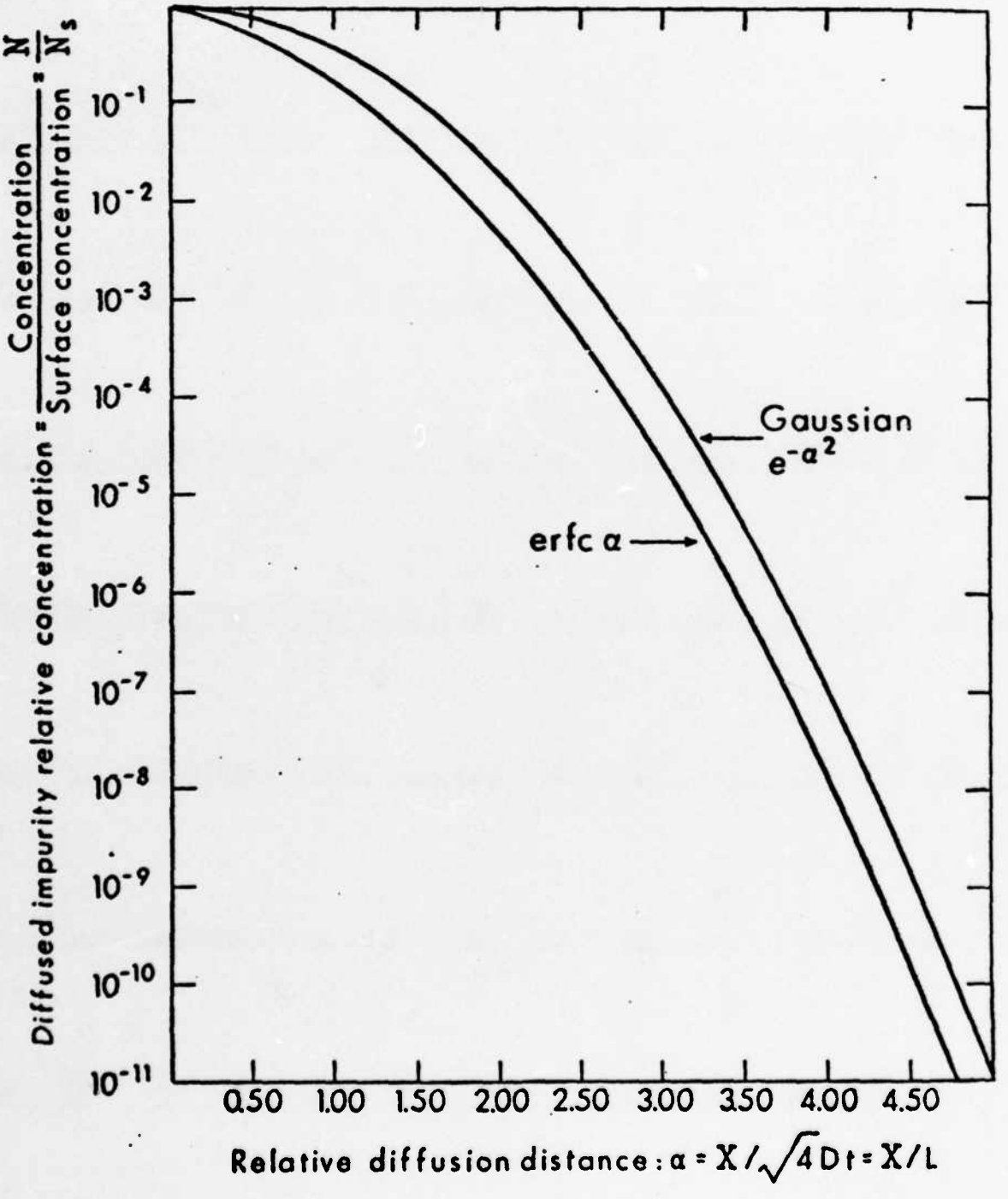

Figure 3.9. Normalized curves for erfc α and $e^{-\alpha^2}$.

thus ensuring overlap and resultant electrical contact with the inversion layer. The predep was kept light to supress and limit its diffusion during the growth of the gate oxide. After the gate oxide was grown, a heavy phosphorous predep was performed to raise the surface concentration thereby guaranteeing a quality ohmic connection to the drain. To accomplish this, the n^- drain diffusion mask (Fig. 3.4) was used with the negative photoresist procedure to define and open a window in the SiO_2 for the light phosphorous predep (800C, 30 minutes). After a dillute HF etch to remove the P_2O_5 layer the remaining oxide color over the gate was violet $\sim$ 3000Å (App. B). A two hour wet oxidation followed at 1100C to increase the gate oxide thickness to $\sim$ 10,000Å (Fig. 1.3) resulting in a violet oxide $\sim$ 1.05 μm or 0.86 μm (App. B). (The thick oxide was to provide for a homogeneous conduction channel thickness at relatively high injection current.) The substrate and drain contact mask (Fig. 3.5) was used (negative photoresist procedure App. A) to define and etch windows in the SiO_2 followed by a 15 minute, 950C phosphorous predep for the n^+ substrate and drain electrical contact. A dillute HF etch removed the P_2O_5 glass. A violet $\sim$ 1000Å (App. B) blocking oxide was then grown (15 minutes, 1000C wet oxidation). A window in the SiO_2 for the base contact diffusion was defined and etched (negative photoresist procedure) using the mask shown in Fig. 3.6. A 15 minute 950C boron predep was then performed to improve the quality of the base contact. After B_2O_3 glass removal (dillute HF etch) a $\sim$ 1000Å blocking oxide was grown (15 minute, 1000C, wet O_2). Windows in the SiO_2

were defined and open with the negative photoresist procedure using the metallization contact mask (Fig. 3.7). These windows provide for electrical contact between the aluminum and the substrate, base, and drain contact diffusions. Aluminum was evaporated at 8×10^{-7} torr and was defined with the metallization mask (Fig. 3.8) and the positive photoresist procedure (App. A).

The MOSBJT was characterized using a Tektronix Type 576 curve tracer as illustrated in Fig. 3.10. The MOSBJT bipolar junction transistor characteristics as a function of gate voltage is shown in Fig. 3.11. For a constant gate voltage and base current, the collector current gradually increases as the collector (drain)-emitter (substrate) voltage increases. This effect was much more pronounced at large gate voltages and probably results from the collection of electron-hole pairs generated in the reverse biased drain/base junction and in the depletion region under the gate. Increases in gate voltage or drain to emitter voltage enlarges the depletion region volume and therefore increases the total number of electron-hole pairs thermally generated in this volume and therefore the number of electrons collected by the reverse biased inversion layer and drain contact thereby resulting in an increased collector current.

The MOSBJT bipolar junction transistor characteristics reveals a similar dependence on gate voltage as the MOSFET with bipolar source (Sec. 1.2). The device gain and value at which the collector current saturates increases as the gate voltage is increased, probably due to the increase in the inversion layer density (discussed in Sec. 1.2).

The maximum BJT gain of ~ 0.8 is probably a result of low injection efficiency (substrate/base junction) resulting from a graded base concentration which is greater than the emitter concentration. The reverse BJT characteristics (in which the substrate is the collector and the drain the emitter) shown in Fig. 3.12 displayed a gain of ~ 200. This is consistent with a favorable injection efficiency of the emitter (drain)/base junction.

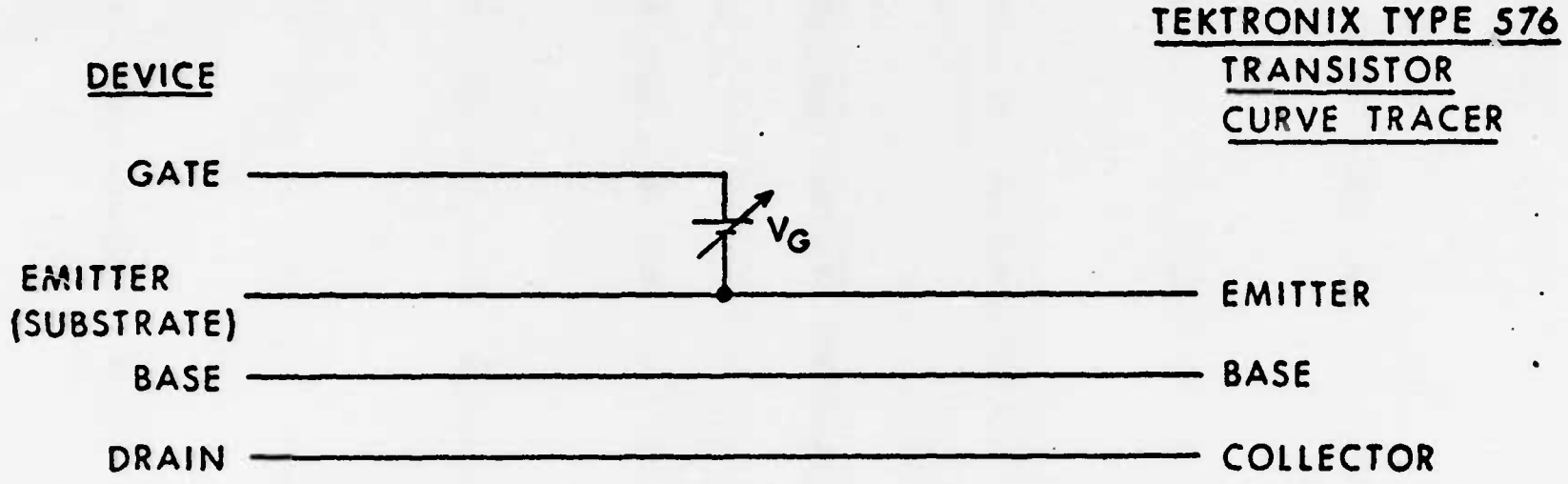

Figure 3.10. Test circuit configuration for the MOSBJT fabricated with a diffused base.

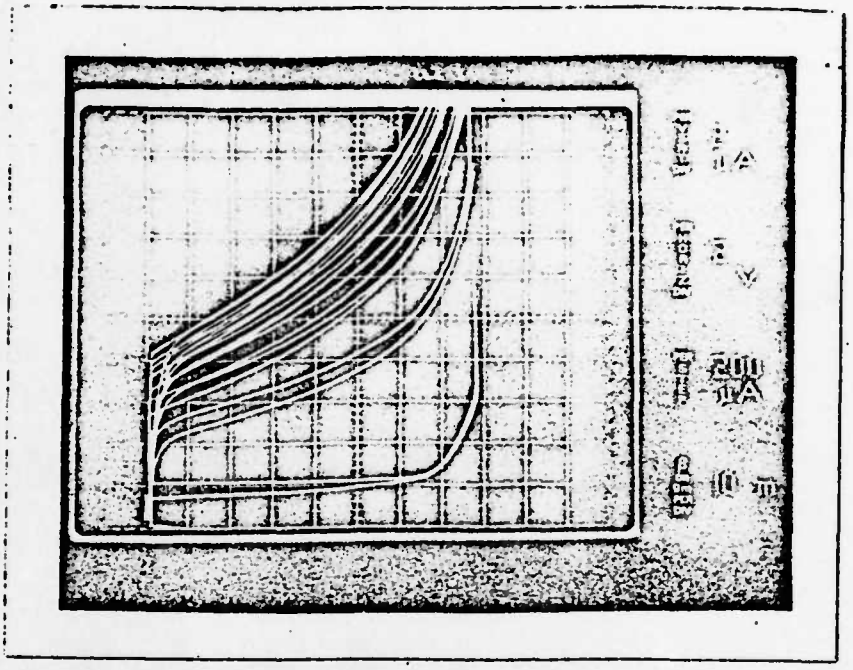

Fig. 3.11a. V_G = -10V

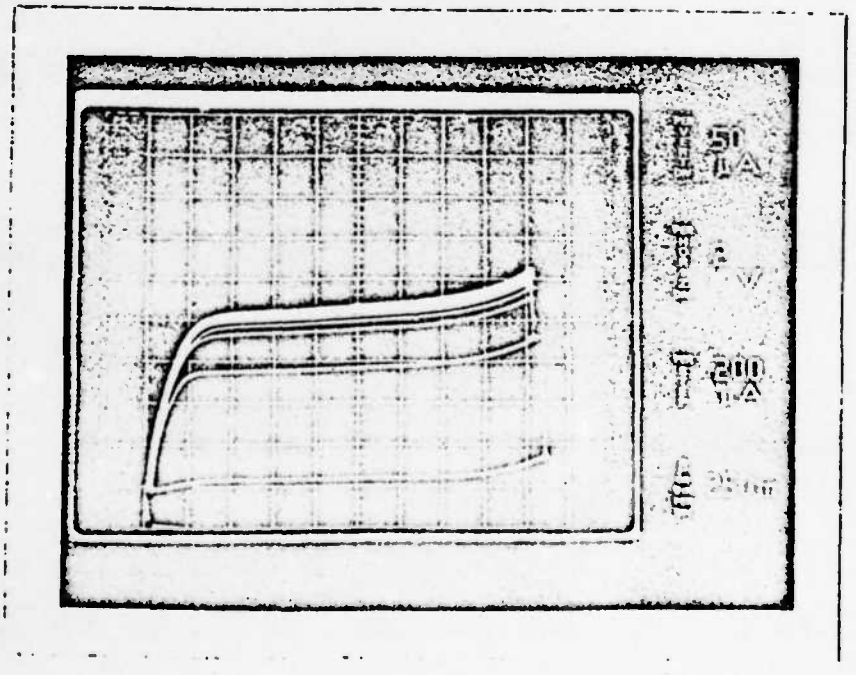

Fig. 3.11b. V_G = +10V

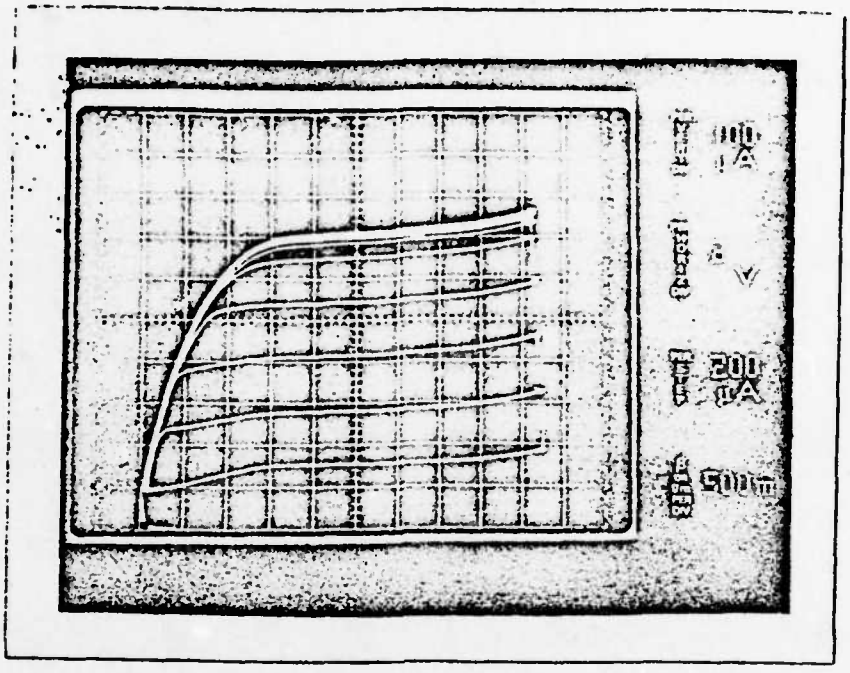

Fig. 3.11c. V_G = 20V

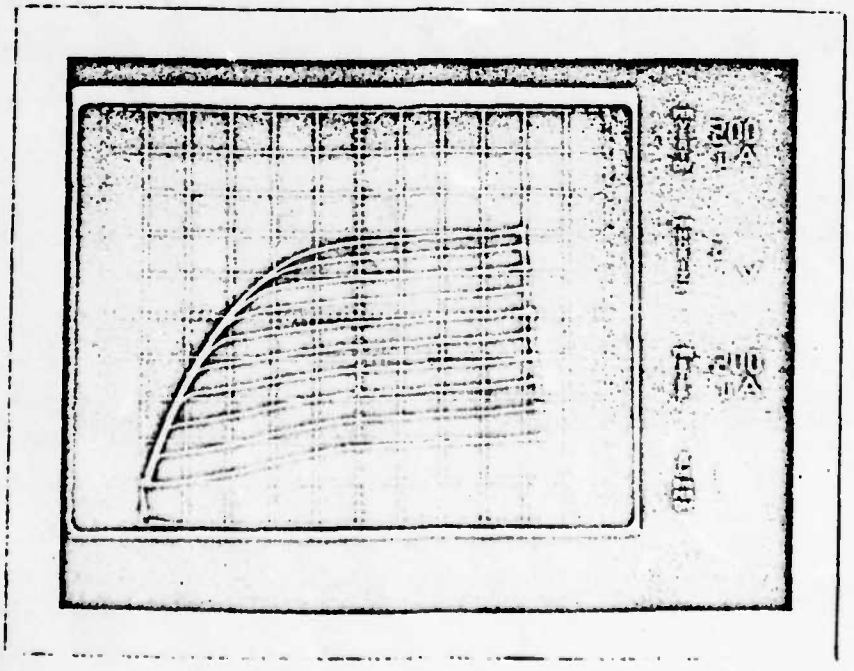

Fig. 3.11d. V_G = 30V

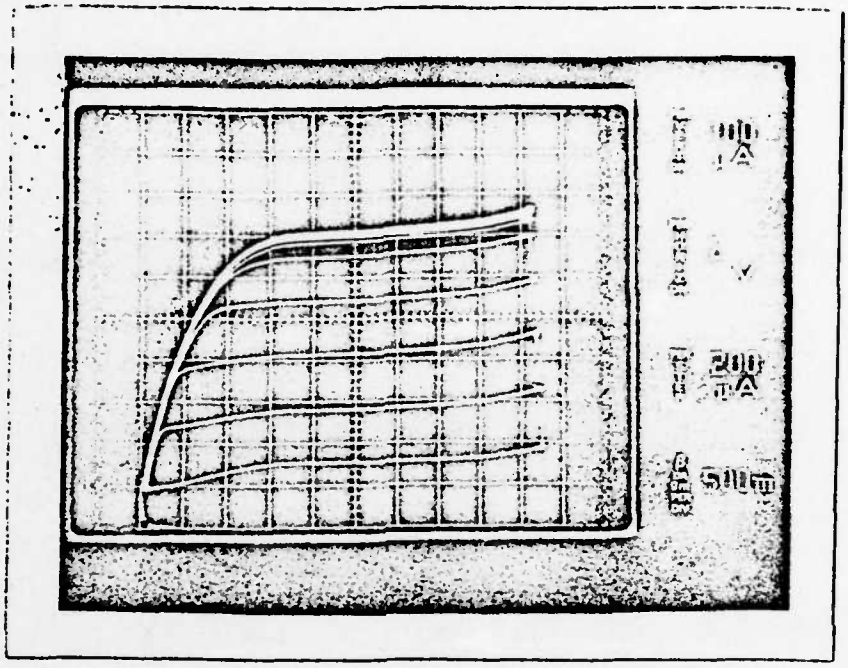

Fig. 3.11c. V_G = 20V

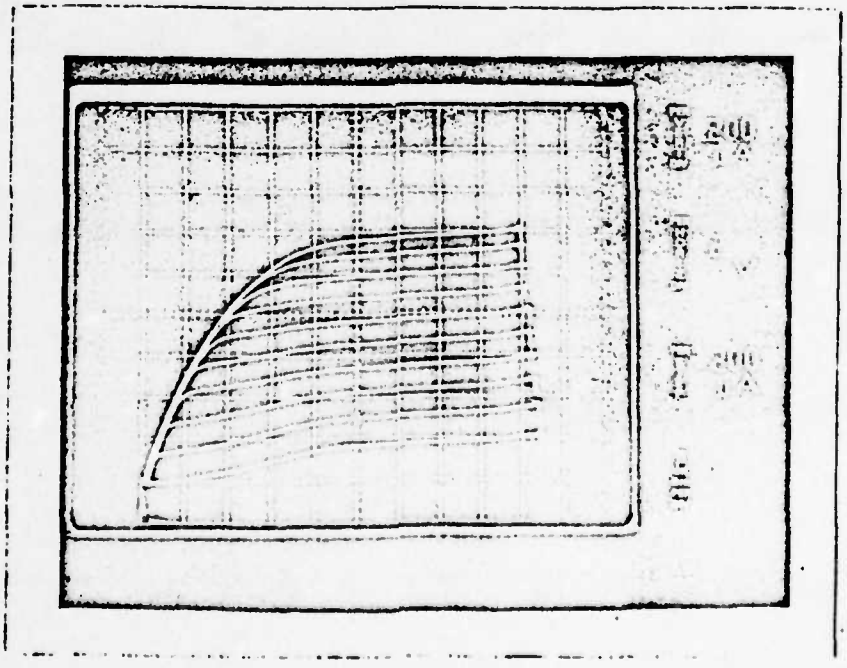

Fig. 3.11d. V_G = 30V

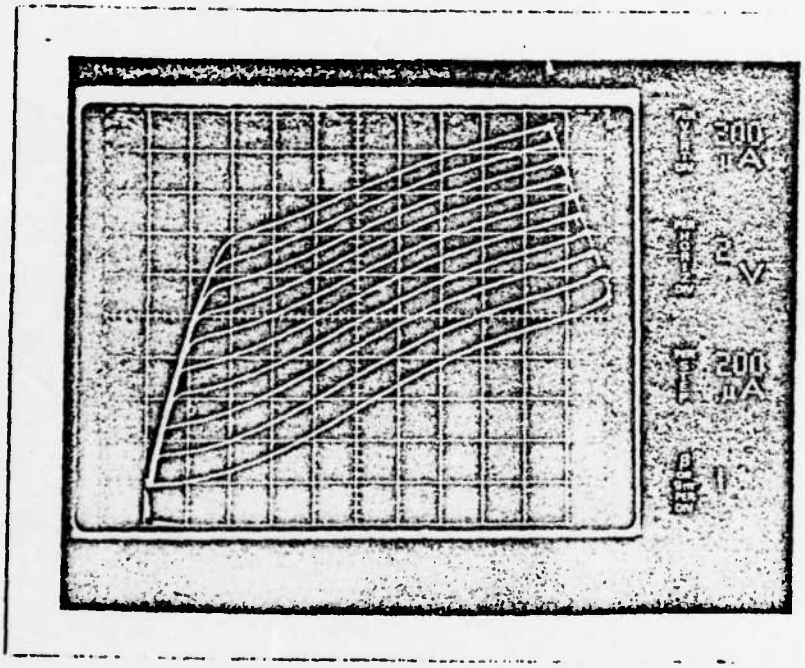

Fig. 3.11e. V_G = 50V

Figure 3.11. MOSBJT (diffused base) BJT characteristics as a function of gate voltage. Gate oxide is ∿ 10,000Å.

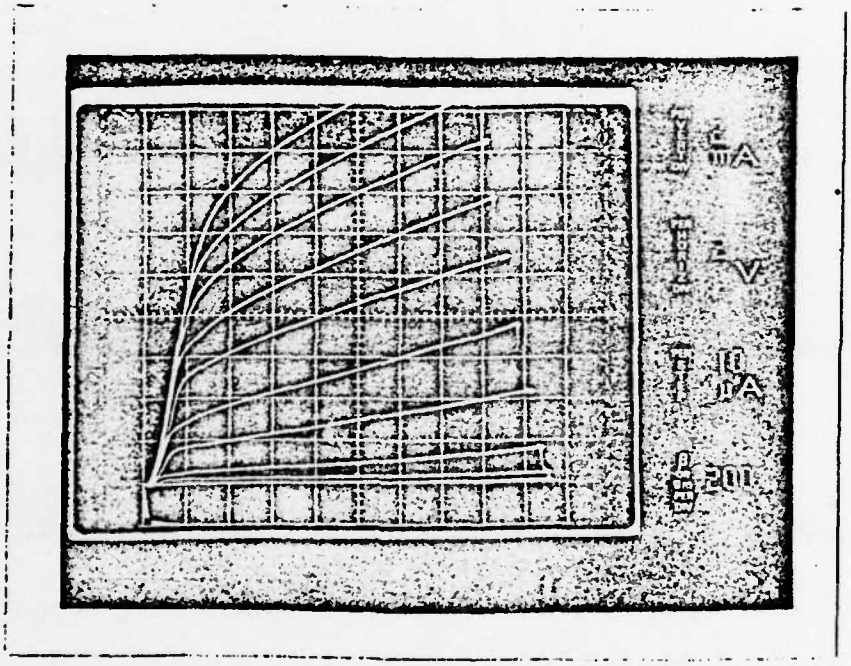

Figure 3.12. MOSBJT (diffused base) "reverse" BJT characteristics.

2.4 MOSBJT Having an Epitaxial Base and a Diffused Isolation Region

To provide gain in an MOSBJT, consideration of a concentration design constraint was necessary. This constraint was met by growing a 10 μm, 1 Ω-cm p-type epitaxial layer on a n^+ substrate (Fig. 4.1) in place of the p region diffused into the n substrate for the previous device. This improved the injection efficiency of the base-substrate junction and reduced current crowding effects within the base. To aid the future analysis of the MOSBJT, two sets of devices were fabricated. A processing schedule was devised to produce devices with 1000Å and 10,000Å gate oxides while maintaining identical temperature/time histories (assumes identical diffusion environments).

The silicon wafers were antimony-doped (100) oriented substrate with a 1 Ω-cm 10 μm thick epitaxial layer. The resistivity of the epitaxial layer was measured with four point probe measurements (Table 4.1), which indicated an average resistivity of ∿ 1.0 Ω-cm (Eqs. 2.4, 2.5).

The fabrication procedure was as follows: The wafers were cleaned (App. A) and a ∿ 5000Å oxide (blue) was grown with a 90 minute wet oxidation process (Fig. 1.3). The negative photoresist procedure (App. A) and the isolation mask (Fig. 3.3) was used to define and etch an oxide window. Using the normalized erfc curve (Fig. 3.9), it was established that a 7 hour 1150C phosphorous predep was appropriate. The wafers were given a HF dip to remove the P_2O_5 glass and negative photoresist was used to etch the n^- diffusion window (Fig. 3.4). A phosphorous predep was performed at 800C for 15 minutes to provide an

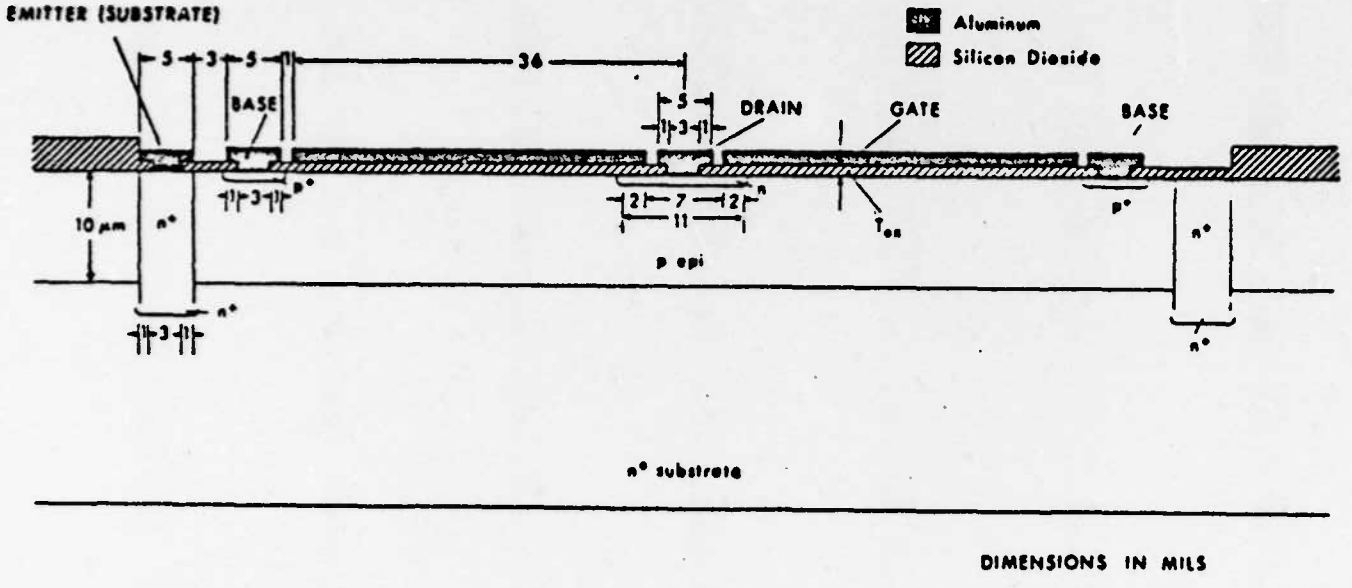

Figure 4.1. Cross sectional view of a MOSBJT with an epitaxial base.

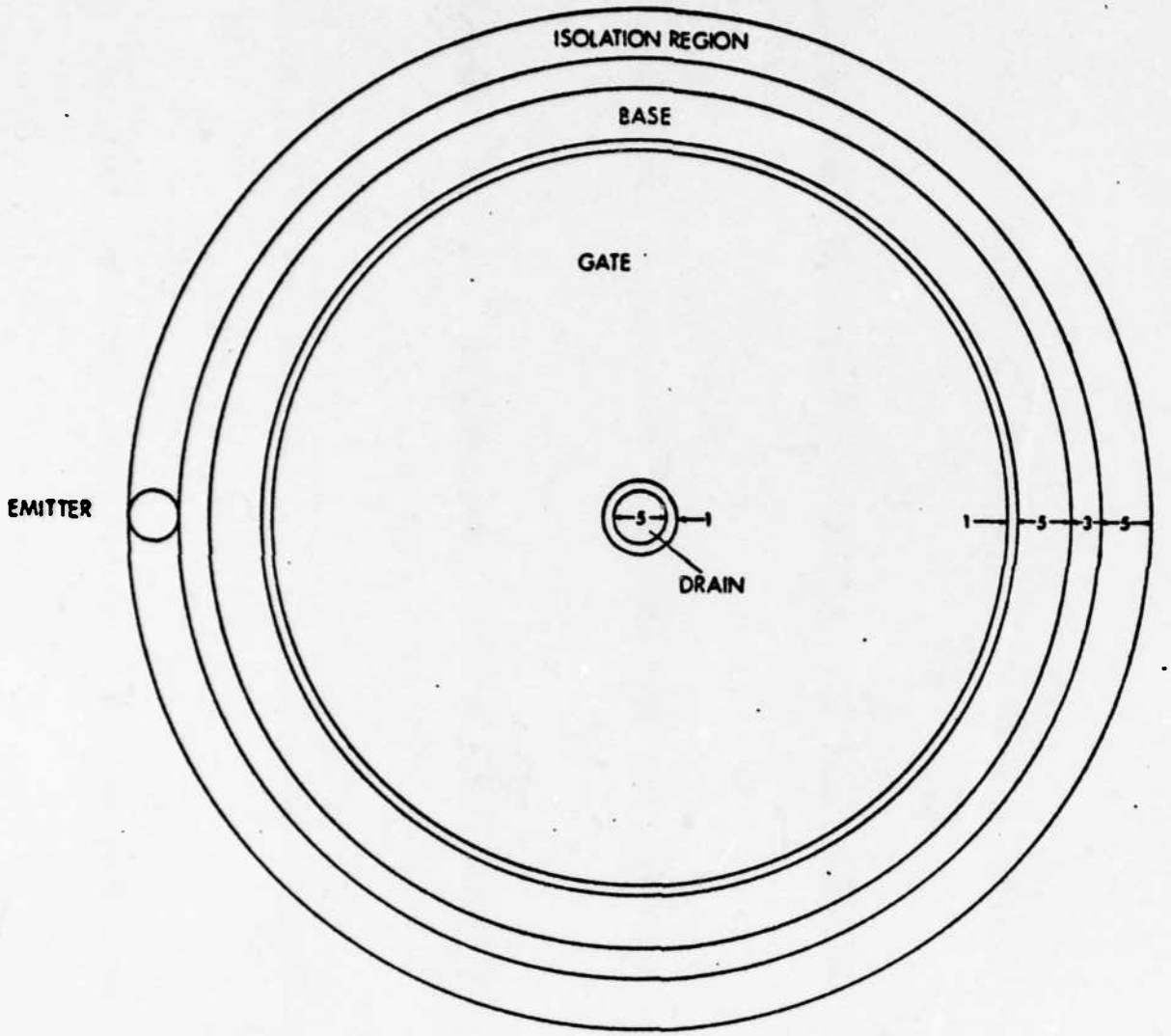

Figure 4.2. Top view of an MOSBJT with an epitaxial base.

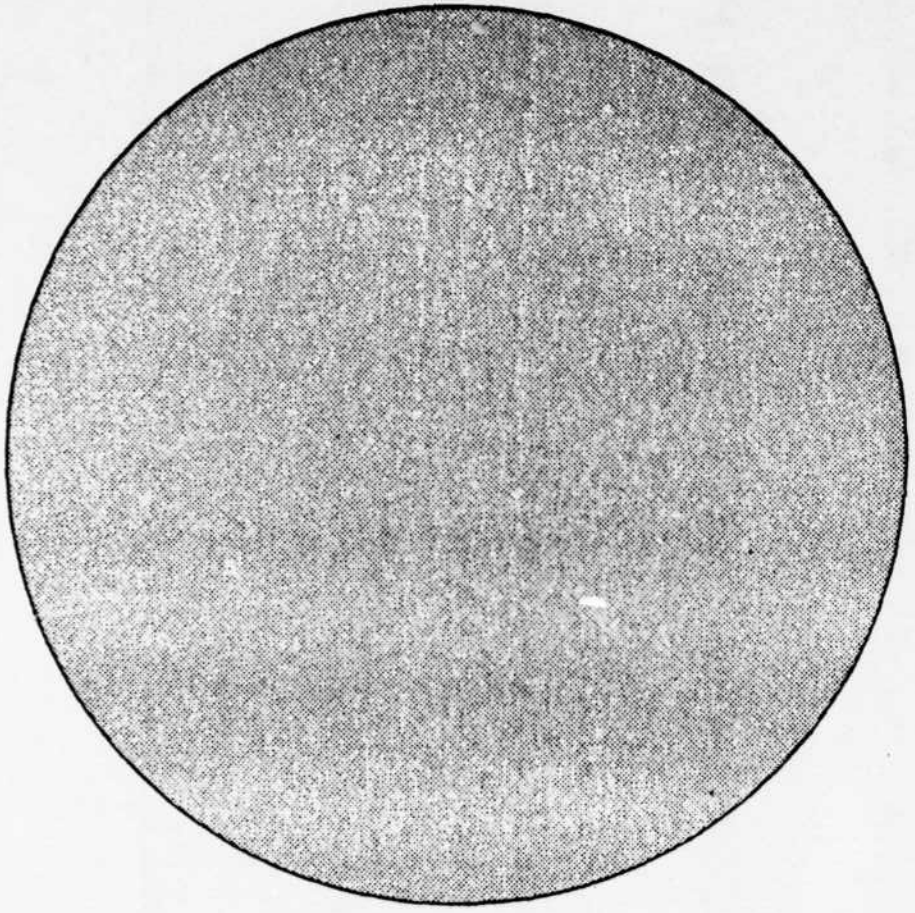

Figure 4.3. Gate oxide regrowth mask.

TABLE 4.1

Four point probe measurements of epitaxial layer

I (mA)	V/I (Ω)	ρ (Ω-cm)
0.5	240	1.1
0.5	250	1.1
0.5	260	1.2
0.5	210	1.0
1.0	210	1.0
1.0	210	1.0

electrical contact to the inverted MOS channel.

The existing oxide over the gate region was removed using the negative photoresist procedure (App. A) and the gate oxide regrowth mask (Fig. 4.3). For the 10,000Å gate oxide device a 2 hour 5 minute 1100C wet oxidation (Fig. 1.3) was completed resulting in a violet oxide ∿ 10,000Å (App. B). The thin (1000Å) oxide was grown in two steps in order to expose the device to the same thermal history as the thick (10,000Å) oxide device and also to consume an equal amount of silicon in its growth, resulting in identical base dimensions: First a wet oxide was grown for 1 hour and 55 minutes at 1150C and then removed with the negative photoresist procedure (App. A) using the gate oxide regrowth mask (Fig. 4.3); A 10 minute 1150C wet oxidation process followed resulting in a violet oxide ∿ 1000Å thick (App. B).

The substrate and drain contact diffusion windows (Fig. 3.5) were opened using negative photoresist and a phosphorous predep was performed at 950C for 15 minutes to provide the n^+ contact regions. The P_2O_5 glass was removed with a dillute HF etch and a blocking wet oxide was grown over the contact windows (15 minutes, 1000C). The resulting gate oxides were violet (∿ 10,000Å) and blue (∿ 1200Å) (App. B).

Negative photoresist was used with the base contact diffusion mask (Fig. 3.6) to define and etch a window in the SiO_2 for a boron predep, 950C for 15 minutes and 10 minutes, for the 10,000Å and 1000Å oxide devices, respectively. The B_2O_3 glass was removed with a dillute HF etch and a blocking wet oxide was grown for 12 minutes at 1000C followed by a 45 minute N_2 anneal at 1000C to reduce the surface state

concentration [2]. The results were violet ($\sim$ 10,000Å) and blue ($\sim$ 1200Å App. B) gate oxides. The metallization contact window mask (Fig. 3.7) was used to define and etch windows in the oxide and aluminum was evaporated at 8×10^{-7} torr. The metallization was defined with positive photoresist (App. A) and the metallization mask (Fig. 3.8).

This MOSBJT fabricated with an epitaxial base was characterized using a Tektronix 576 curve tracer (Fig. 4.4). The effect of gate voltage on the BJT characteristics of the 1200Å and 10,000Å devices are displayed in Figs. 4.5 and 4.7, respectively. Compared to the previous MOSBJT devices (Sec. 2.3) the maximum gain increased to $\sim$ 1, probably the result of the favorable injection efficiency of the base (epitaxial layer)/emitter (substrate) junction. A factor that may be degrading the base/emitter injection efficiency is the interdiffusion of the antimony from the n^+ substrate into the base during the high temperature processes forming a graded junction. The reverse BJT characteristics illustrated in Figs. 4.6 and 4.8 reveal a gain of $\sim$ 50 and 20. This is lower than the MOSBJT fabricated with a diffused base and could result from the reduction of the base minority carrier diffusion length due to recombination lifetime degradation caused by defects such as stacking faults or dislocations in the epitaxial layer.

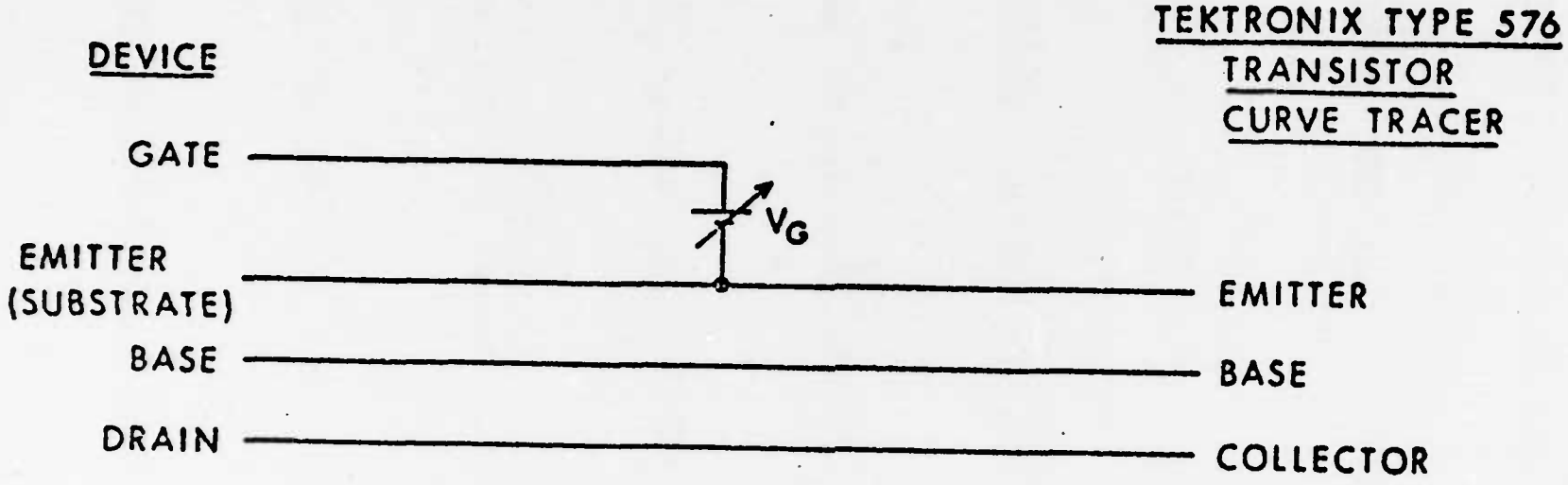

Figure 4.4. Test circuit used for the MOSBJT having an epitaxial base.

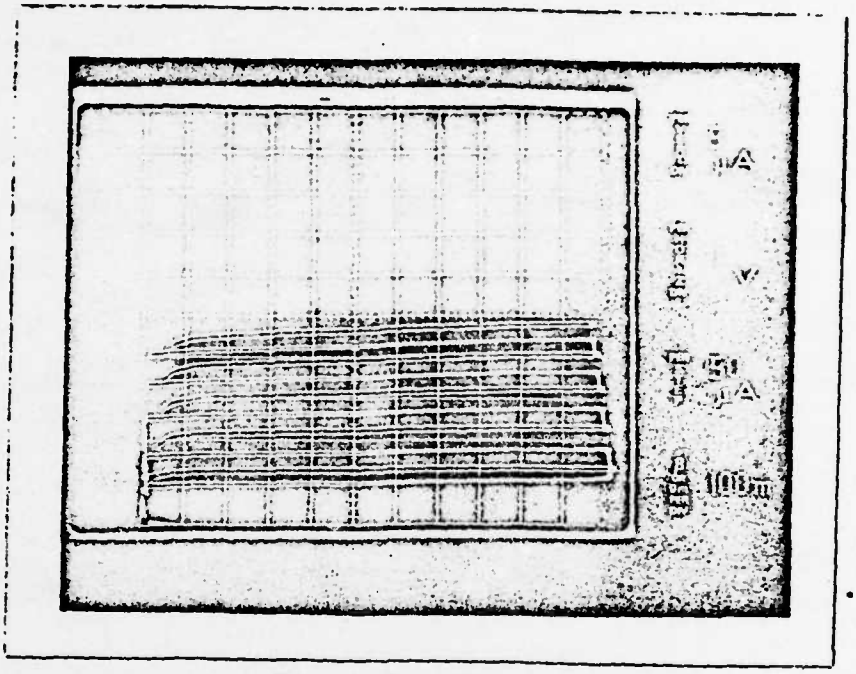

Fig. 4.5a. V_G = -5V.

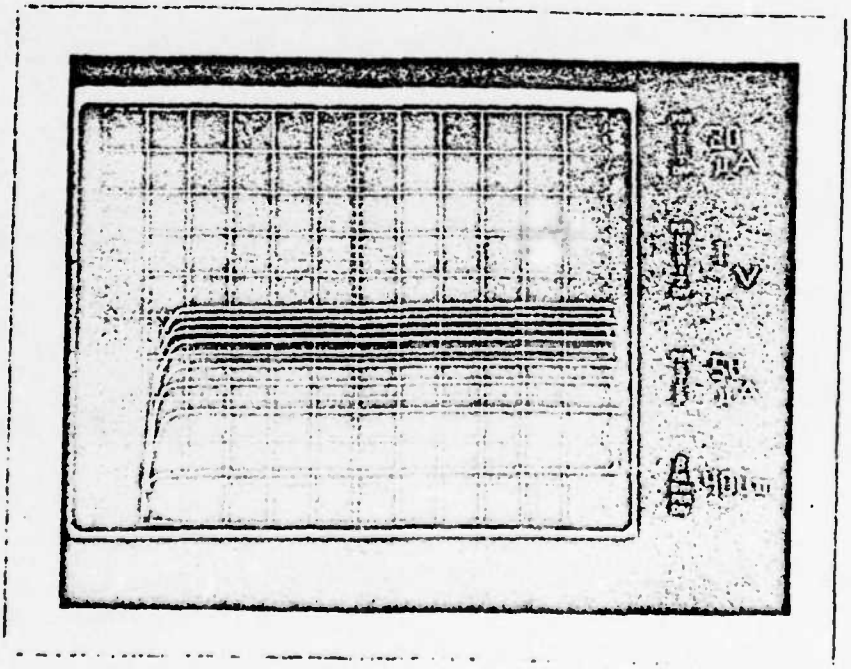

Fig. 4.5b. V_G = 0V.

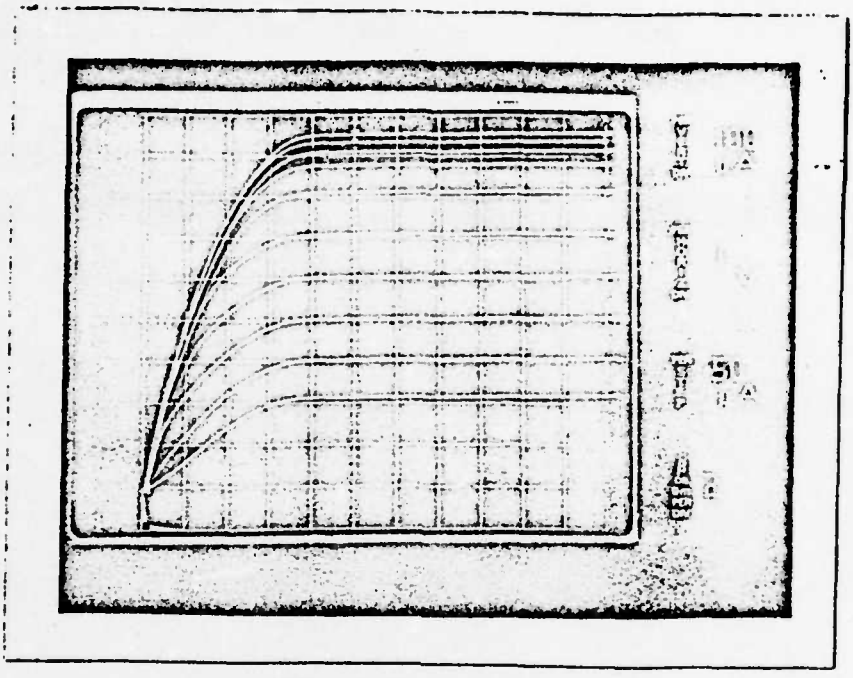

Fig. 4.5c. V_G = 5V.

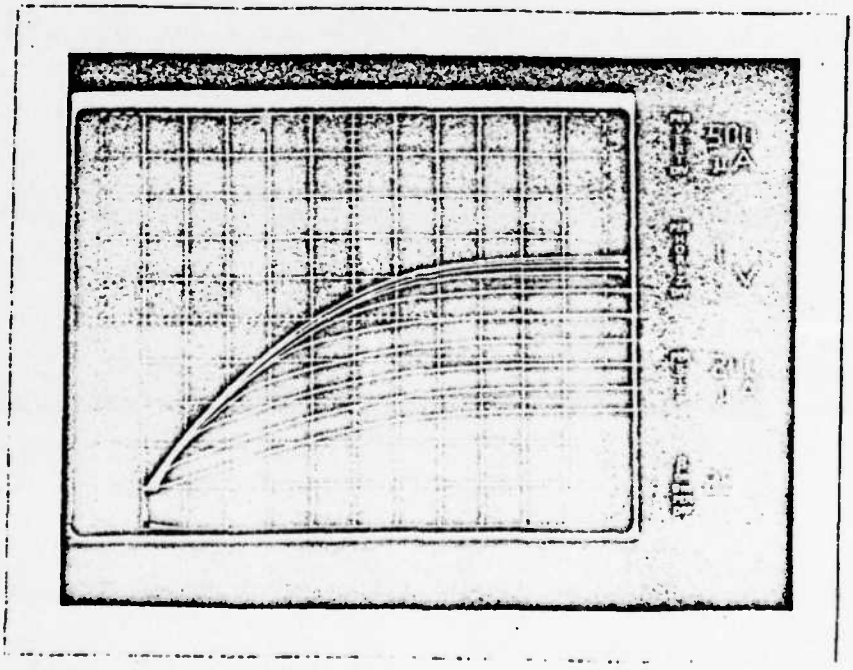

Fig. 4.5d. V_G = 10V.

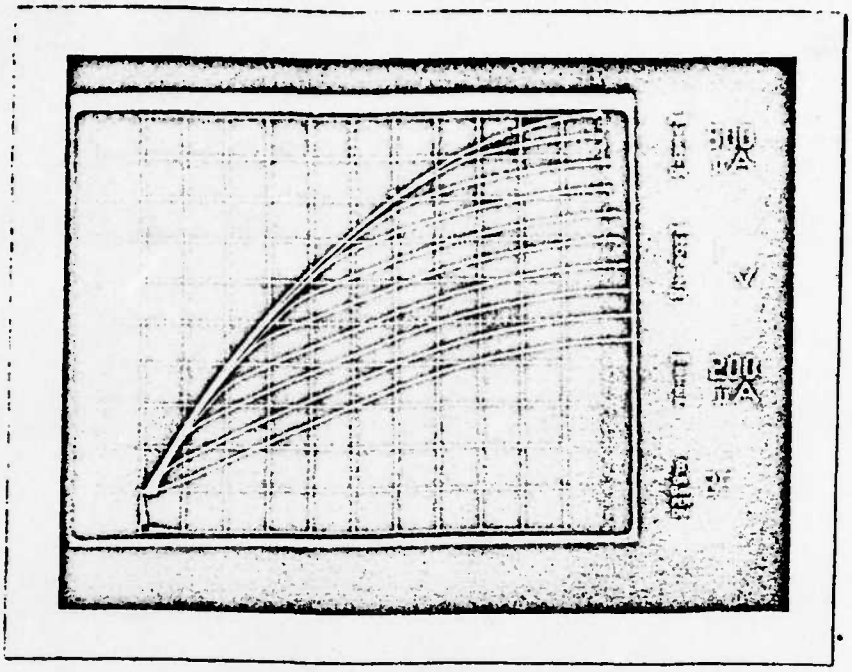

Fig. 4.5e. V_G = 15V.

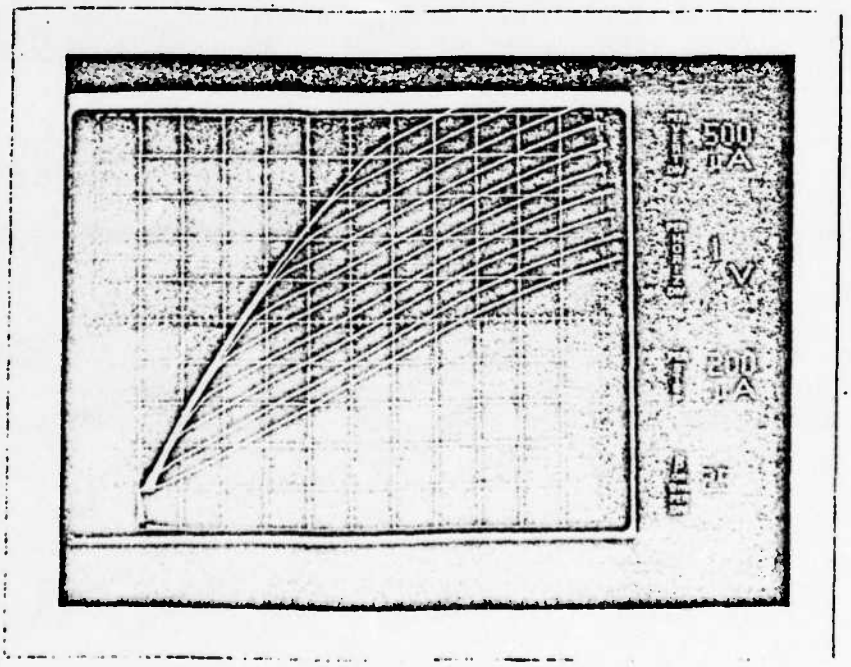

Fig. 4.5f. V_G = 20V.

Figure 4.5. MOSBJT (epitaxial base) BJT characteristics as a function of gate voltage. Gate oxide is 1200Å.

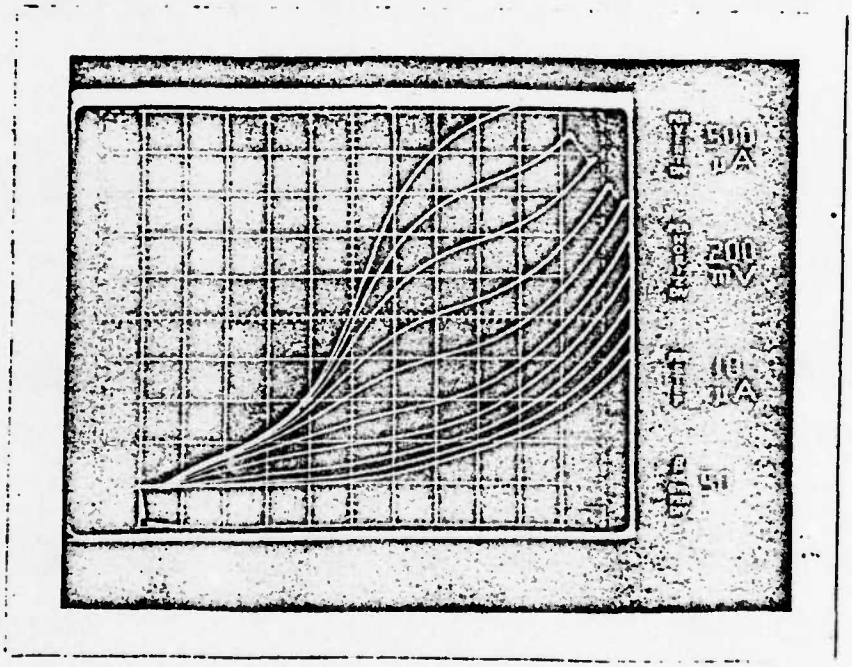

Figure 4.6. MOSBJT (epitaxial base) reverse BJT characteristics. Gate oxide is 1200Å.

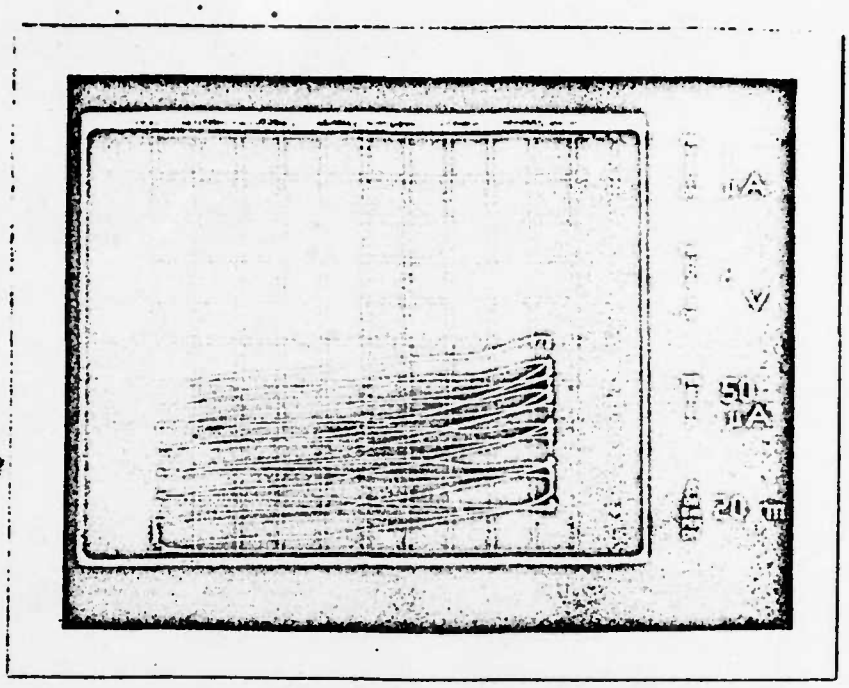

Fig. 4.7a. V_G = 0V.

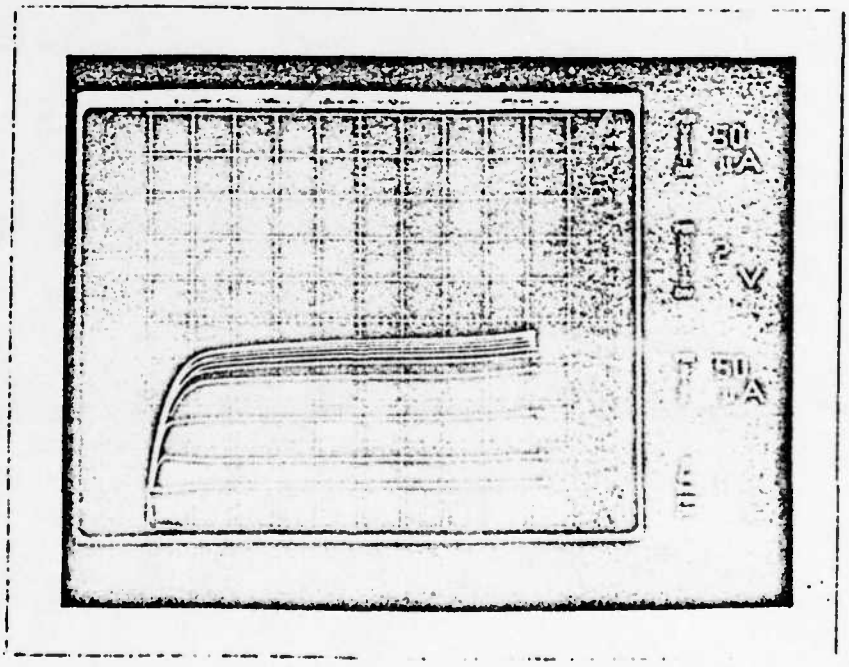

Fig. 4.7b. V_G = 10V.

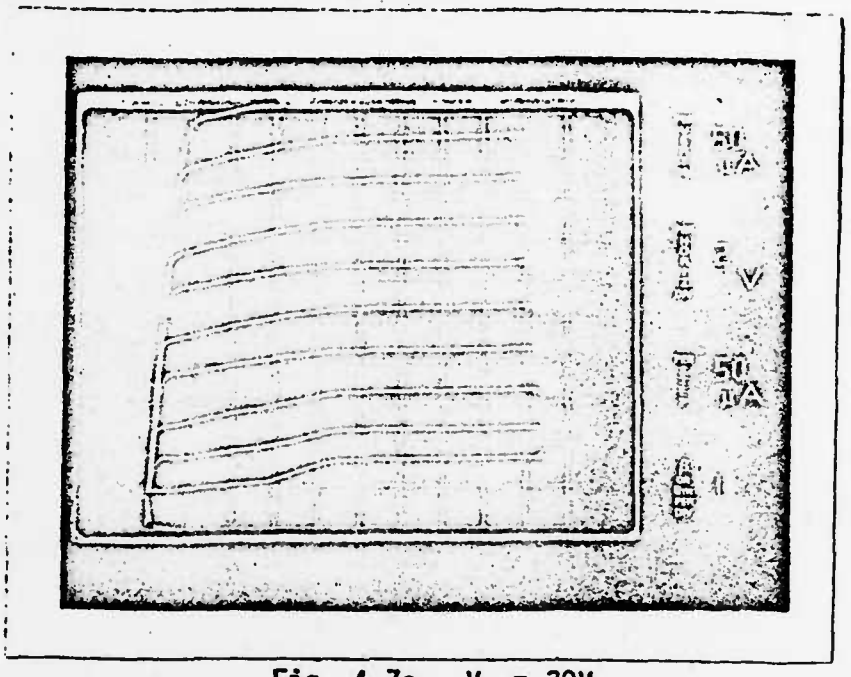

Fig. 4.7c. V_G = 30V.

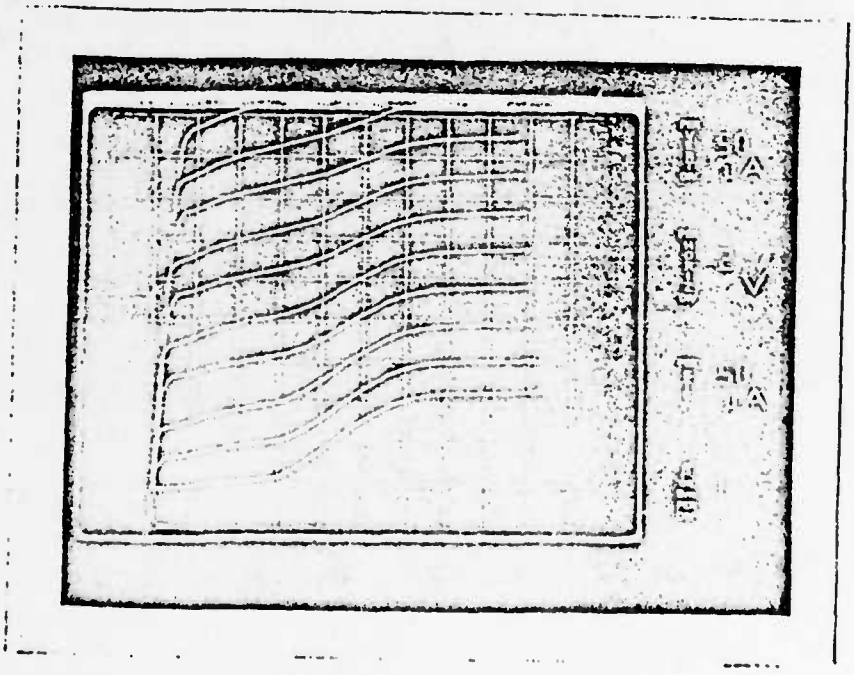

Fig. 4.7d. V_G = 40V.

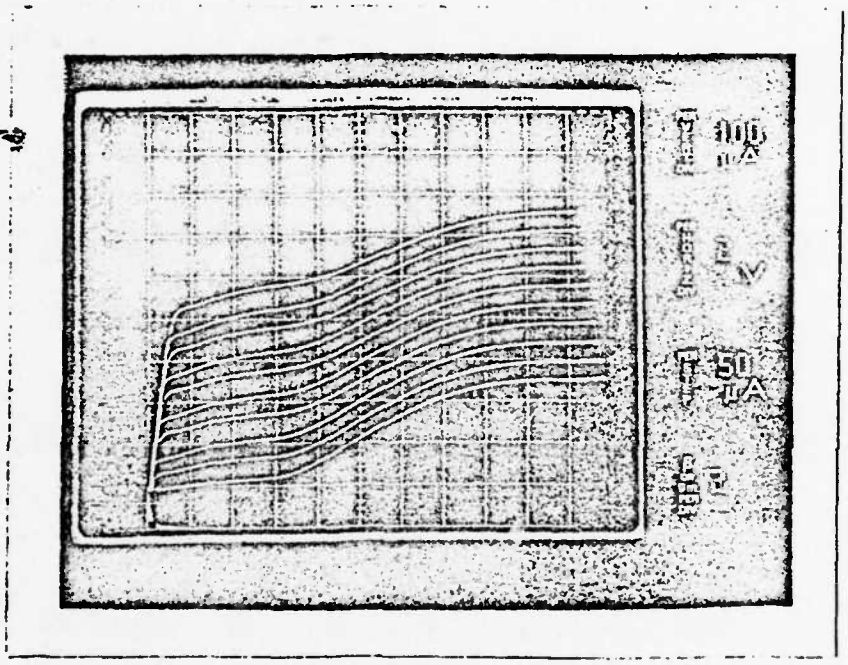

Fig. 4.7e. V_G = 50V.

Figure 4.7. MOSBJT (epitaxial base) BJT characteristics as a function of gate voltage. Gate oxide is 10,000Å.

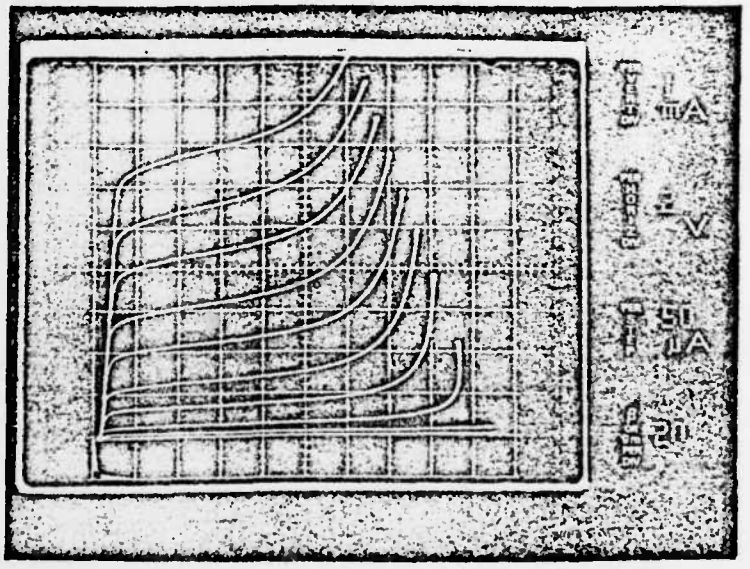

Figure 4.8. MOSBJT (epitaxial base) reverse BJT characteristics. Gate oxide is 10,000Å.

2.5 MOSBJT Having an Epitaxial Base and a Mesa Etched Isolation Region

One cause of the low gain in the previous MOSBJTs is probably the diffusion of antimony from the substrate into the base epitaxial layer degrading the injection efficiency of the base-substrate junction. To reduce the Sb diffusion and thereby increase the gain, devices were fabricated with an etched isolation region (Fig. 5.2), eliminating the long isolation diffusion and relative high temperature processing.

The (100) oriented silicon wafers consisted of a 10μm, 1 Ω-cm resistivity, p-type epitaxial layer grown on a n^+ antimony-doped substrate. To etch the 10μm deep isolation ring the negative photoresist procedure (App. A) was followed except that CP-4 was used instead of buffered HF. CP-4's chemical activity varies with temperature and from batch to batch and required testing to determine whether the photoresist could withstand the etchant and to characterize the etch rate. To decrease the activity of the CP-4, it was dilluted 10:1::CP-4:DI. A test silicon wafer was etched and measurements with a micrometer established that a 3 minute etch was sufficient to remove 10μm of silicon. Before the wafers were etched, negative photoresist was used to protect the back of the wafer from the etchant, reducing the heating and undesirable increase in chemical activity of the CP-4. Device isolation was verified when I-V characteristics between the central regions of two isolation rings were "back to back" diode characteristics. These characteristics result from the p-epitaxial layer/n^+ substrate/p-epitaxial layer structure that occurs when the isolation ring etches through the epitaxial layer.

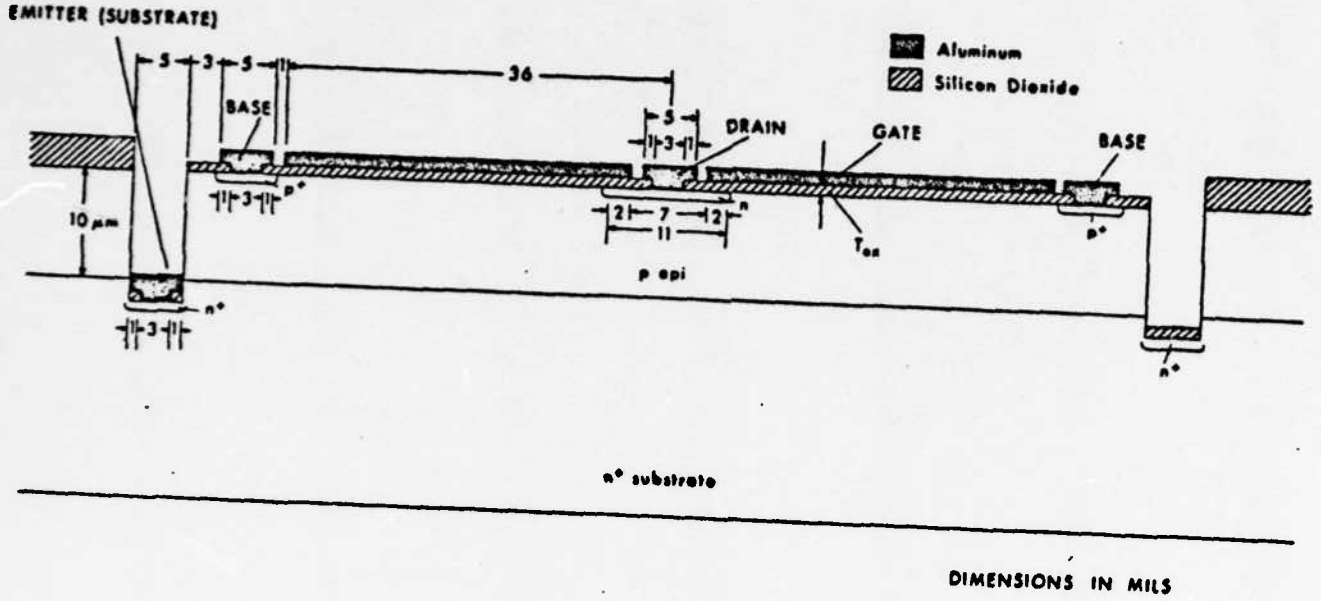

Figure 5.1. Cross sectional view of MOSBJT with an etched isolation ring.

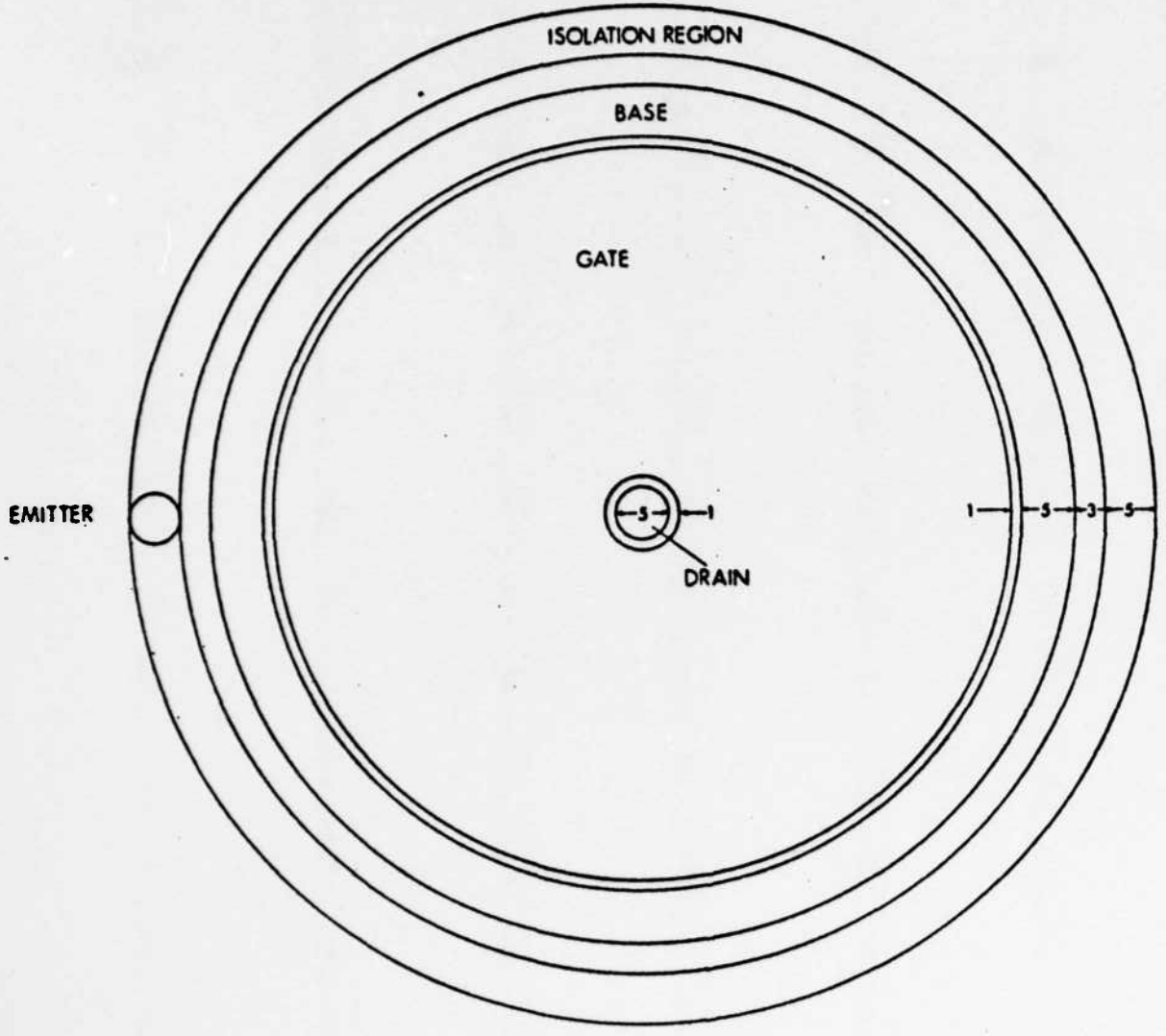

Figure 5.2. Top view of MOSBJT with an etched isolation ring.

The remaining fabrication of the 1000Å gate oxide devices proceeded as follows. The wafers were cleaned (App. A) and a 90 minute 1000C wet oxide grown. The negative photoresist procedure was used with the n^- drain diffusion mask (Fig. 3.4) and isolation mask (Fig. 3.3) to define and etch windows in the oxide. A phosphorous predep was performed at 950C for 15 minutes. The P_2O_5 glass was removed with a dillute HF and a 15 minute 1000C wet blocking oxide was grown. The base contact diffusion mask (Fig. 3.7) was used in the negative photoresist procedure (App. A) to open windows in the oxide for a 15 minute 950C boron predep. The existing oxide over the gate region was removed (gate oxide regrowth mask--Fig. 4.3, negative photoresist procedure). The gate oxide was grown dry at 1000C for 100 minutes and nitrogen annealed [2]. The resulting gate oxide color was royal blue corresponding to 1200Å (App. B). Negative photoresist was used to define and etch the drain, base, and substrate metallization contact windows (Fig. 3.8). Aluminum was evaporated at 8×10^{-7} torr and metal pads defined (positive photoresist, App. A, metallization mask, Fig. 3.8).

Fabrication procedure for the 10,000Å MOSBJT was as follows. Identical wafers were used. The isolation ring was etched in the same manner as the previous 1200Å oxide devices. A blocking oxide (wet, 90 minute, 1000C) was grown resulting in a royal blue color corresponding to $\sim$ 4900Å (App. B). The n^- drain diffusion mask (Fig. 3.4) and the isolation mask (Fig. 3.3) were used to etch windows in the oxide for a 15 minute 800C phosphorous predep. The existing oxide over the gate was removed (negative photoresist, App. A, gate oxide regrowth mask,

Fig. 4.3) and the gate oxide was grown wet for 2 hours and 5 minutes at 1100C ($\sim$ 10,000Å, Fig. 1.3). The substrate and drain contact diffusion windows (Fig. 3.5) were defined and etched (negative photoresist, App. A) and a 950C, 15 minute phosphorous predep was performed to provide the n^+ substrate and drain contact regions. The P_2O_5 glass was removed with a dillute HF etch and a wet oxide was grown for 15 minutes at 1000C. To ensure that the aluminum forms a good ohmic contact with the p epitaxial layer, the base contact window (Fig. 6) was defined using negative photoresist, etched, and a 15 minute, 950C boron predep performed. Dillute HF removed the B_2O_3 and a wet blocking oxide was grown for 15 minutes at 1000C. The negative photoresist procedure was used to define and etch the metallization contact windows (Fig. 3.7) and aluminum was evaporated at 8×10^{-7} torr. The metallization was defined with postive photoresist and the metallization mask (Fig. 3.8).

The MOSBJT fabricated with an epitaxial base and mesa etched isolation region was characterized with a Tektronix 576 curve tracer in the circuit shown in Fig. 5.3. The effect gate voltage has on the BJT characteristics is revealed in Figs. 5.4 and 5.6 for the 1200Å and 10,000Å devices, respectively. The maximum gain was $\sim$ 3 for the 1200Å device and $\sim$ 2 for the 10,000Å device. The gain of these devices are slightly larger than the MOSBJT with a diffused isolation region probably the result of the elimination of the isolation diffusion. This reduces the degree of interdiffusion of antimony into the epitaxial layer and therefore probably increases the injection efficiency of the

emitter/base junction. The relatively slight increase in gain resulting from the reduction of a significant amount of high temperature processing implies that the interdiffusion of antimony into the base may not be the major cause of the low gain of the MOSBJT.

The reverse BJT characteristics of the device was observed by using the drain as the emitter and the substrate as the collector. The reverse characteristics of the 1200Å and the 10,000Å devices shown in Figs. 5.5 and 5.6 reveal a gain of 50 and 25, respectively. The consistent low reverse gain of the MOSBJT devices with an epitaxial base layer indicates that the epitaxial layer may be the major cause of the low gain. As mentioned previously this may be caused by a short minority carrier lifetime in the base epitaxial layer due to recombination of defects. Also lattice strain at the forward biased epitaxial layer (base)/substrate (emitter) interface may be causing substantial amount of recombination which would result in a large increase in base current and therefore a significant reduction in gain.

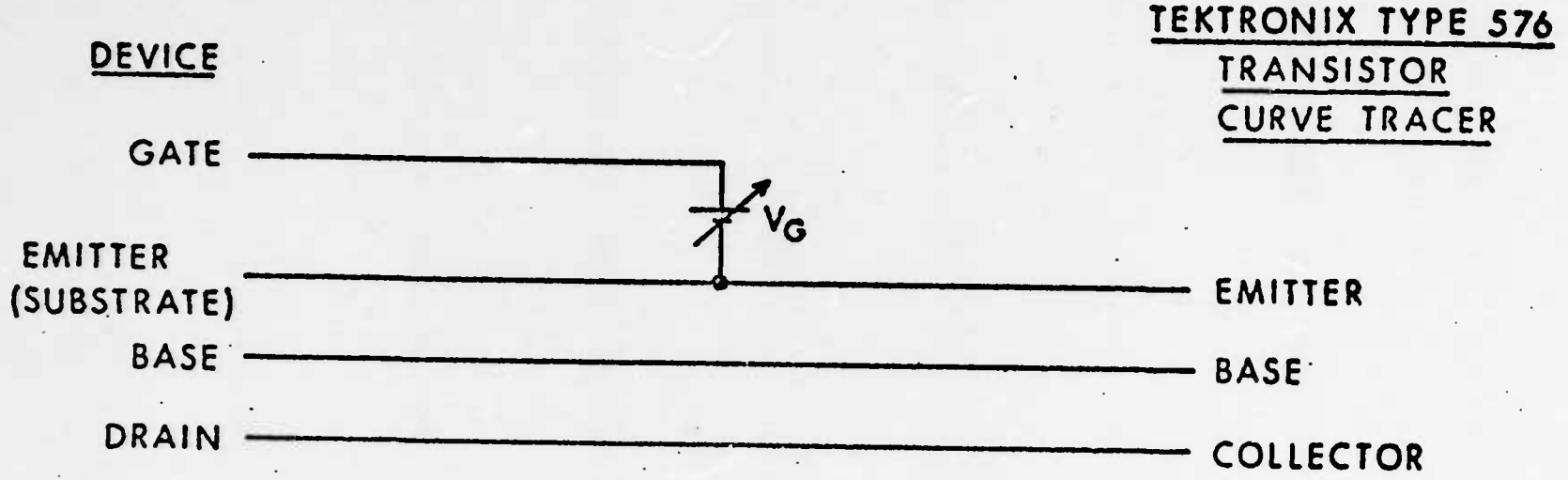

Figure 5.3. Test circuit configuration for the MOSBJT having an epitaxial base and a mesa etched isolation region.

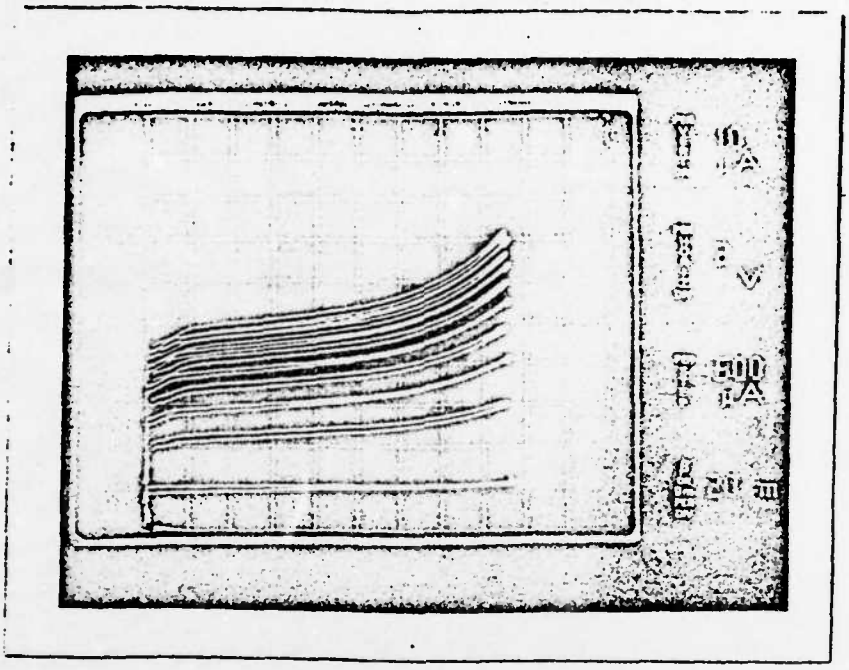

Fig. 5.4a.. V_G = 0V.

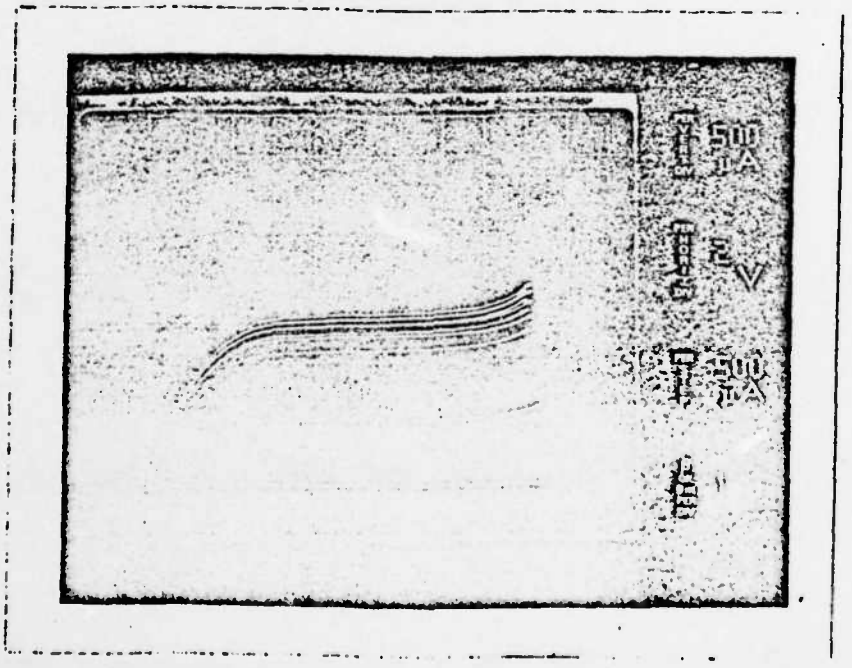

Fig. 5.4b. V_G = 10V.

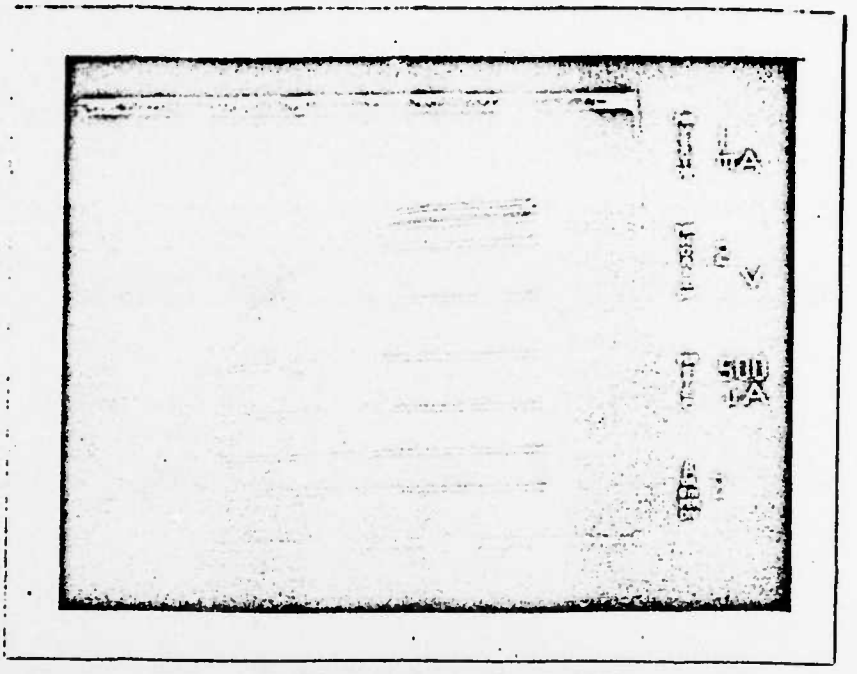

Fig. 5.4c. V_G = 20V.

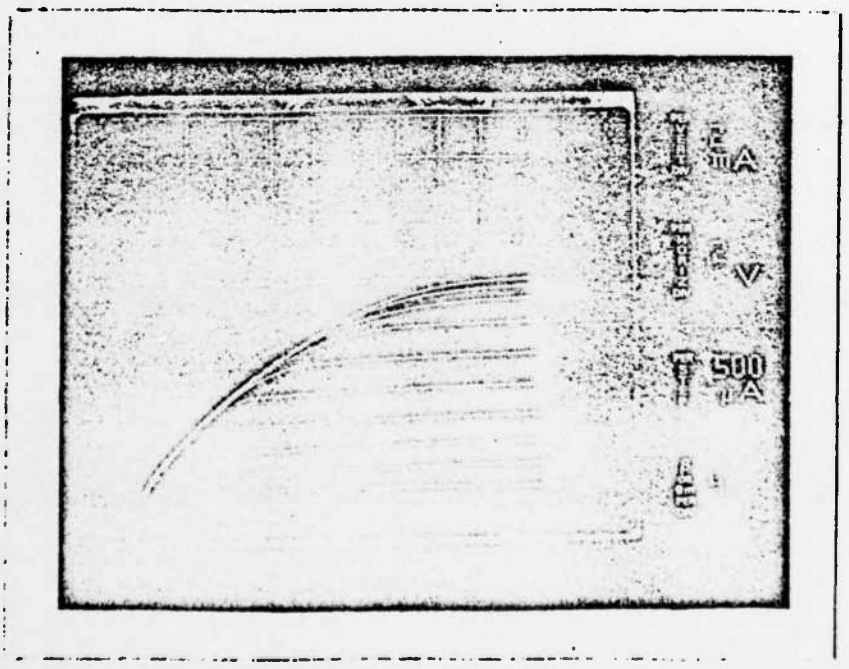

Fig. 5.4d. V_G = 25V.

Figure 5.4. MOSBJT (epitaxial base, mesa etched isolation) BJT characteristics as a function of gate voltage. Gate oxide is 1200Å.

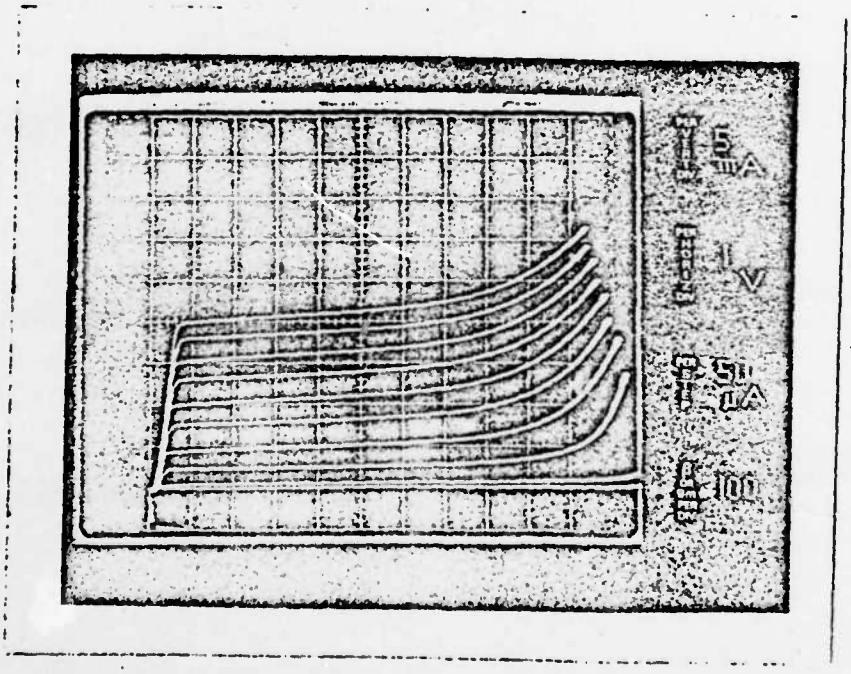

Figure. 5.5. MOSBJT (epitaxial base, mesa etched isolation) reverse BJT characteristics as a function of gate voltage. Gate oxide is 1200Å.

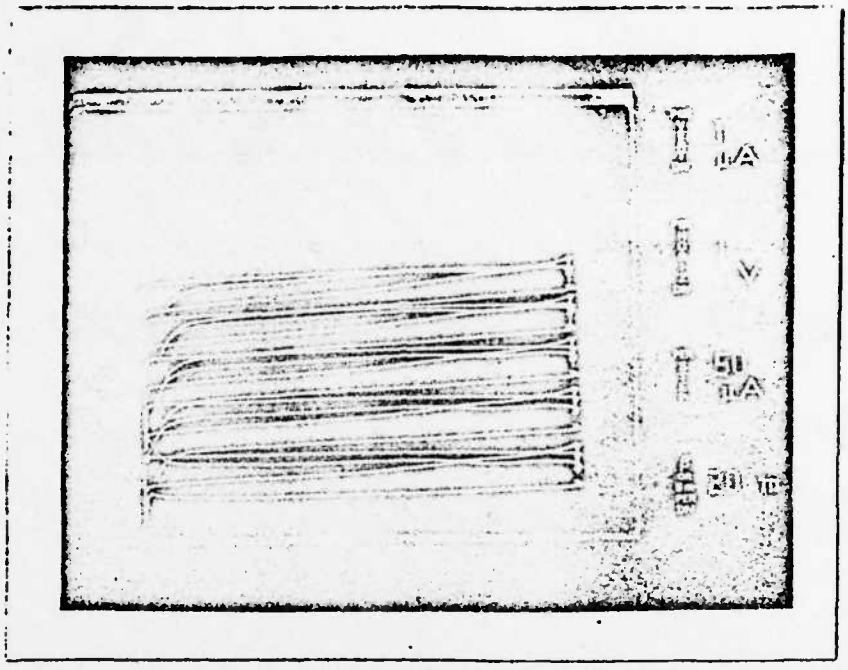

Fig. 5.6a. V_G = negative.

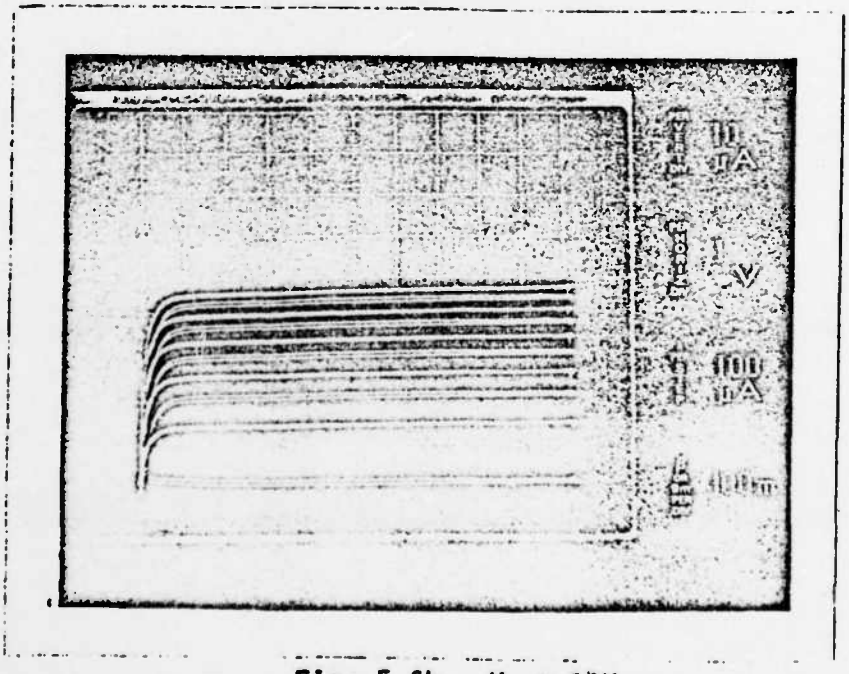

Fig. 5.6b. V_G = 10V.

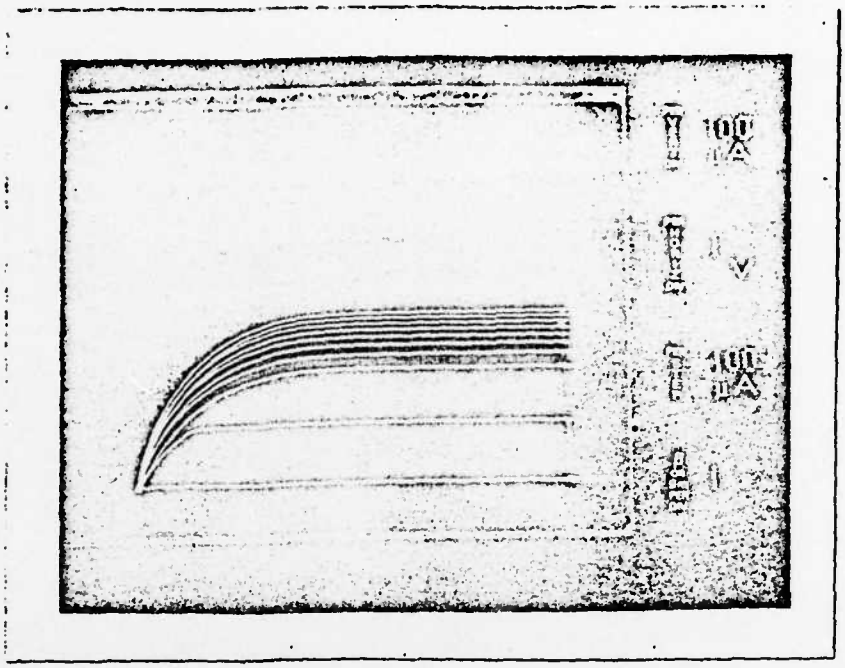

Fig. 5.6c. V_G = 30V.

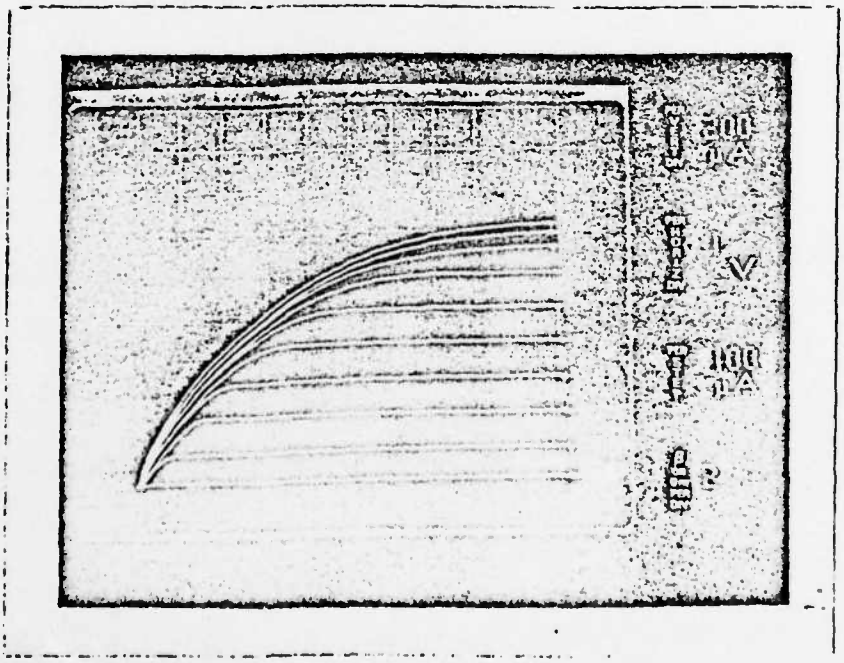

Fig. 5.6d. V_G = 50V.

Figure 5.6. MOSBJT (epitaxial base, mesa etched isolation) BJT characteristics as a function of gate voltage. Gate oxide is $\sim$ 10,000Å.

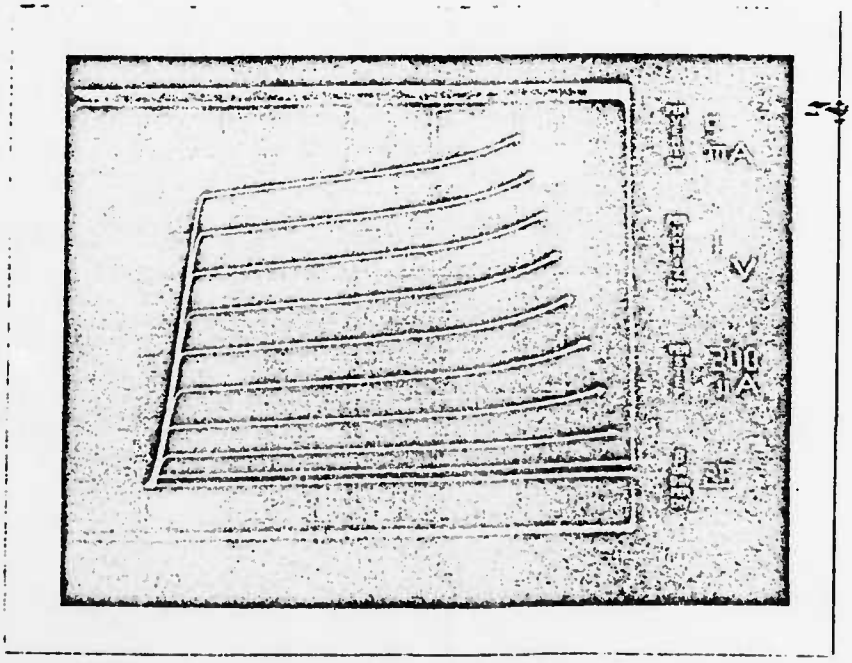

Figure 5.7. MOSBJT (epitaxial base, mesa etched isolation) reverse BJT characteristics as a function of gate voltage. Gate oxide is $\sim 10{,}000\text{Å}$.

AD-A132 332 FABRICATION OF A SILICON MOSFET DEVICE WITH BIPOLAR TRANSISTOR SOURCE(U) HAWAII UNIV AT MANOA HONOLULU DEPT OF ELECTRICAL ENGINEERING D N OKADA JUL 80 2/2

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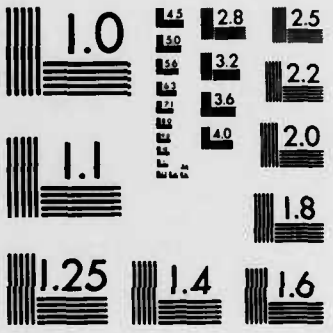


CHAPTER 3

SUMMARY

To verify that MOSFETs of acceptable quality could be fabricated at the University of Hawaii Physical Electronics Lab a MOSFET of a straight forward design was fabricated. The MOSFET was then contructed in a p region diffused into a n substrate. This resulted in a MOSFET with a bipolar souce which had a bipolar gain (β) of $\sim$ 0.3.

A novel device (the MOSBJT) was designed to provide bipolar transistor gain and to confine electron injection into the inverted MOSFET n-channel. The first MOSFET was fabricated with a diffused p-type base region and n^+ isolation region. The maximum bipolar gain of this device was $\sim$ 0.8. A probable cause of the low gain was the poor injection efficiency of the base-emitter junction resulting from a linear graded junction and a heavily doped base region. To increase the injection efficiency of the emitter-base junction the diffused base was replaced by a 1 Ω-cm p-type epitaxial layer grown on a n^+ antimony doped substrate. The bipolar transistor gain of these devices increased to $\sim$ 1.0. To reduce the interdiffusion of the antimony into the epitaxial layer the isolation diffusion was replaced by an etched isolation region. This resulted in the gain increasing to $\sim$ 2.0. The slight improvement in gain of the MOSBJT implies that the low gain is probably not totally due to the degradation of the injection efficiency resulting from the interdiffusion of antimony into the base. The reverse BJT gain (in which the drain is the emitter and the substrate,

the collector) showed a significant decrease in gain for the epitaxial base devices compared with the diffused base devices. This implied that defects such as stacking faults and dislocations may be present in the epitaxial layer and reducing the lifetime in the base. Since the Sb substrate is heavily doped, a substantial defect concentration (recombination centers) in the emitter-base depletion layer is probable. Substantial recombination in the forward biased emitter (substrate)-base (epitaxial layer) junction and within the base could cause a significant increase in base current with a related supression of the gain. The final device goals were achieved with the MOSBJT in which a MOSFET and BJT were successfully integrated while maintaining satisfactory gain with a substantial controlled injection into the inverted MOSFET channel.

At this time experiments for which the MOSBJT was conceived are underway.

APPENDIX A

WAFER CLEANING PROCEDURE 1

Process	Time
10:1 HF	10 seconds
DI rinse	2 minutes
H_2SO_4/H_2O_2	5 minutes
DI rinse	5 minutes
DI rinse	5 minutes
N_2 Blow Dry	

WAFER CLEANING PROCEDURE 2

Process	Time
10:1 HF	10 seconds
DI rinse	2 minutes
Ultrasonic agitation and gentle scrubbing in a hot Joy/DI solution	2 minutes
Thorough DI rinse	
H_2SO_4/H_2O_2	5 minutes
DI	5 minutes
DI	10 minutes
Spin dry	

KMER NEGATIVE PHOTORESIST PROCEDURE

Process	Method	Time	Temperature
Coat wafer	Spin at 4000 RPM	15 seconds	Room temperature
Air dry	Under laminar flow hood	3 minutes	Room temperature
Prebake the resist coating		20 minutes	80°C
Expose		6 seconds	
Develop	Immerse in KMER developer	3 minutes	
Rinse	With isopropyl alcohol	3 minutes	
Dry	N_2 blow dry		
Postbake		15 minutes	100°C
Etch the oxide	Buffered HF		
Strip	Using H_2SO_4/H_2O_2 solution		
Clean wafers			

KTI NEGATIVE PHOTORESIST PROCEDURE

Process	Method	Time	Temperature
Coat wafer	Spin at 4000 RPM	15 seconds	Room temperature
Air dry	Under laminar flow hood	3 minutes	
Prebake the resist coating		25 ± 5 minutes	90 ± 5°C
Expose		6 seconds	
Develop	Soak in KTI developer	1 minute	
Rinse	Immerse in KTI rinse	30 seconds	
Dry	N_2 blow dry		
Postbake		25 ± 5 minutes	140°C ± 5°C
Etch the oxide	Buffered HF		
Strip	Using H_2SO_4/H_2O_2 solution		
Clean wafer			

SHIPLEY AZ-1360J POSITIVE PHOTORESIST PROCEDURE

Process	Method	Time	Temperature
Coat wafer	Spin at 4000 RPM	15 seconds	Room temperature
Air dry	Under laminar flow hood	3 minutes	
Prebake the resist coating		15 minutes	100°C
Expose		6 seconds	
Develop	Immerse in AZ-606 developer dilluted 10:1 with DI	25 seconds	
Rinse	In DI	10 seconds	
Dry	N_2 blow dry		
Postbake		15 minutes	95°C
Etch	In 20:1::H_3PO_4:HNO_3		
Strip	Immerse in Shipley remover--1112A dilluted 2:1::DI:1112A	30 seconds	

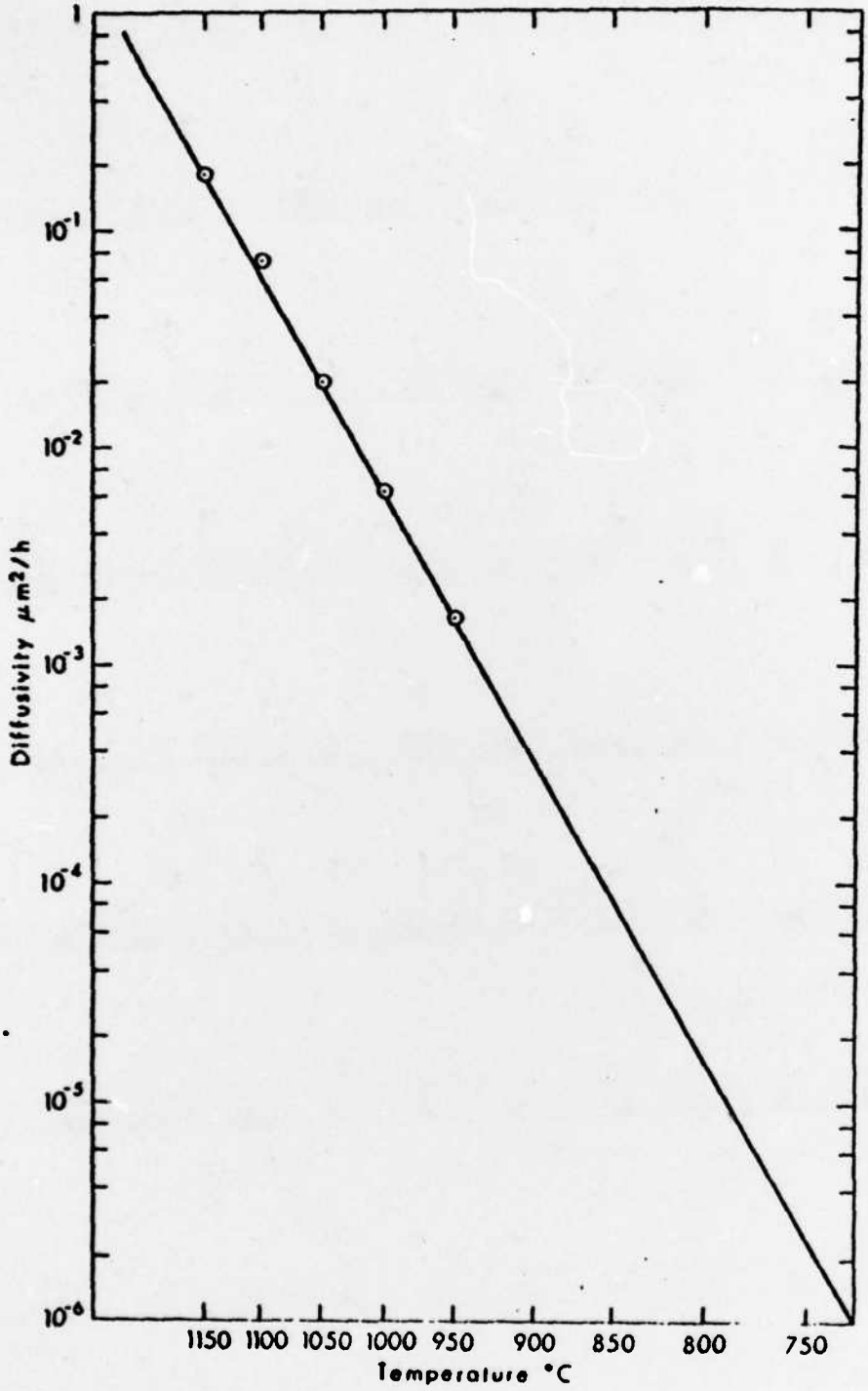
APPENDIX B

SILICON DIOXIDE THICKNESS VS. INTERFERENCE COLOR[7]

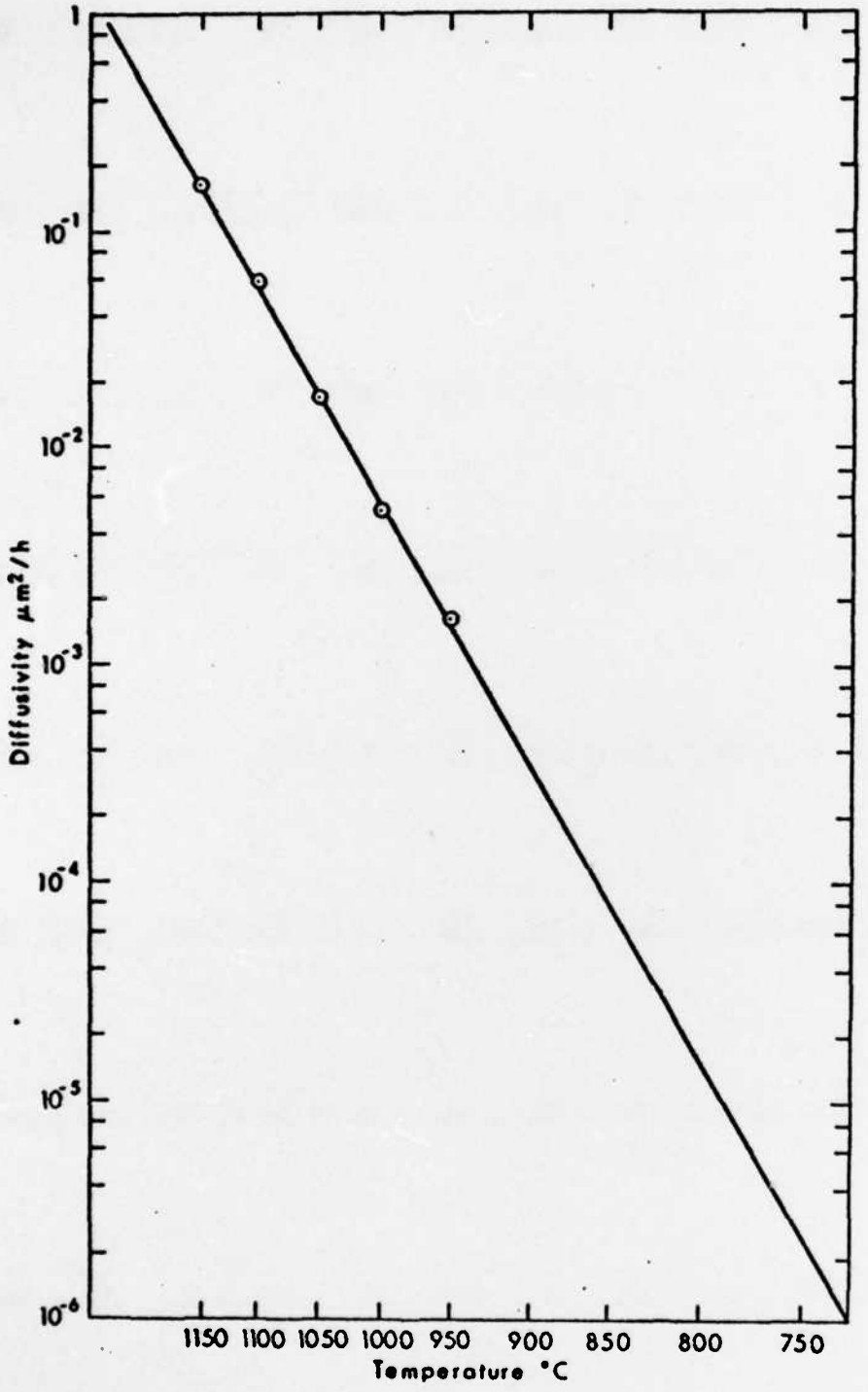
Film Thickness (μ)	Order (5460 A)	Color and Comments
0.05_0		Tan
0.07_5		Brown
0.10_0		Dark violet to red-violet
0.12_5		Royal blue
0.15_0		Light blue to metallic blue
0.17_5	I	Metallic to very light yellow-green
0.20_0		Light gold to yellow - slightly metallic
0.22_5		Gold with slight yellow-orange
0.25_0		Orange to melon
0.27_5		Red-violet
0.30_0		Blue to violet-blue
0.31_0		Blue
0.32_5		Blue to blue-green
0.34_5		Light green
0.35_0		Green to yellow-green
0.36_5	II	Yellow-green
0.37_5		Green-yellow
0.39_0		Yellow

Film Thickness (μ)	Order (5460 A)	Color and Comments
0.41_2		Light orange
0.42_6		Carnation pink
0.44_3		Violet-red
0.46_5		Red-violet
0.47_6		Violet
0.48_0		Blue-violet
0.49_3		Blue
0.50_2		Blue-green
0.52_0		Green (broad)
0.54_0		Yellow-green
0.56_0	III	Green-yellow
0.57_4		Yellow to "yellowish" (Not yellow but is in the position where yellow is to be expected. At times it appears to be light creamy grey or metallic.)
0.58_5		Light-orange or yellow to pink borderline
0.60_0		Carnation pink
0.63_0		Violet-red
0.68_0		"Bluish" (Not blue but borderline between violet and blue-green. It appears more like a mixture between violet-red and blue-green and overall looks greyish.)

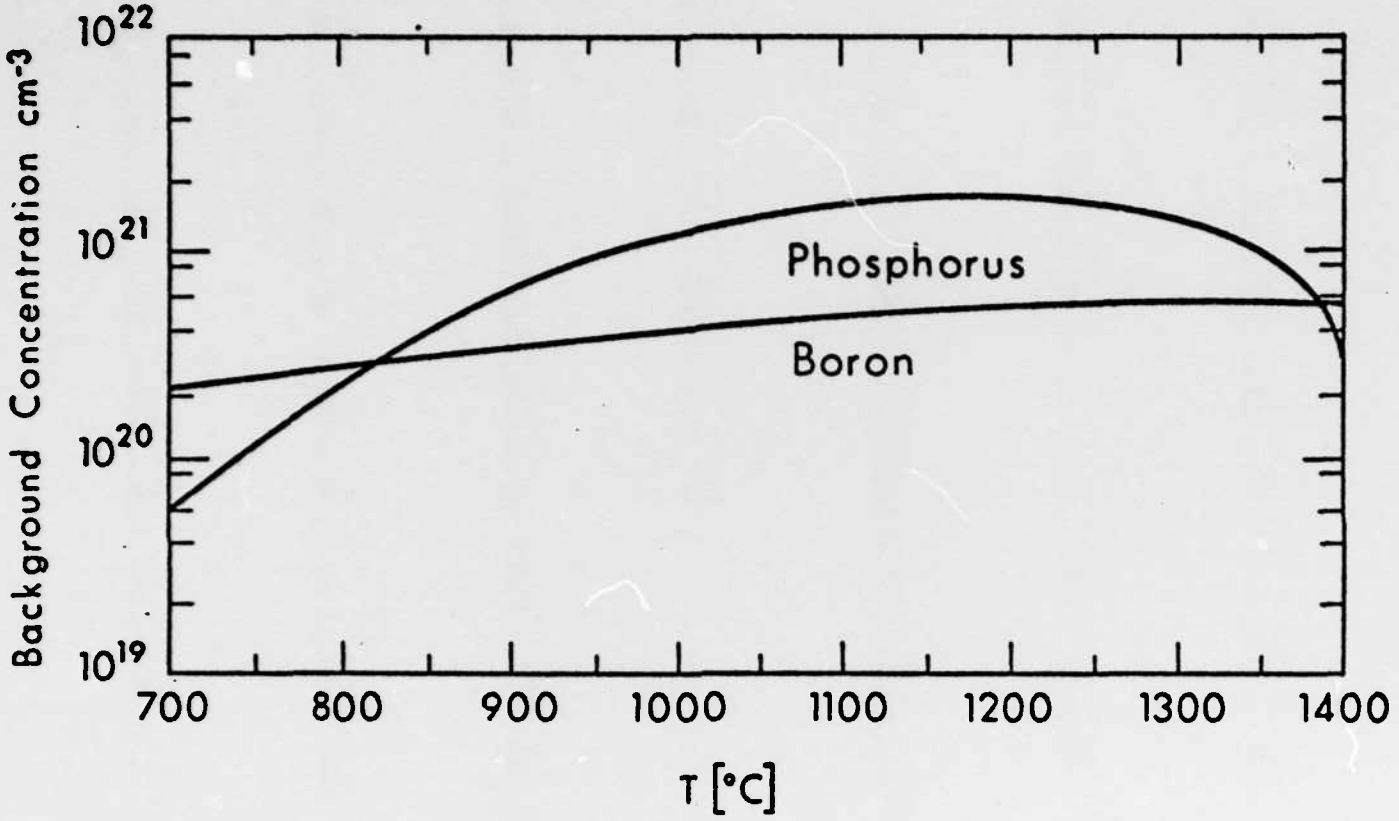
Film Thickness (μ)	Order (5460 A)	Color and Comments
0.72	IV	Blue-green to green (quite broad)
0.77		"Yellowish"
0.80		Orange (rather broad for orange)
0.82		Salmon
0.85		Dull, light red-violet
0.86		Violet
0.87		Blue-violet
0.89		Blue
0.92	V	Blue-green
0.95		Dull yellow-green
0.97		Yellow to "yellowish"
0.99		Orange
1.00		Carnation pink
1.02		Violet-red
1.05		Red-violet
1.06		Violet
1.07		Blue-violet



Phosphorous diffusion coefficient as a function of temperature for silicon.[4]



Boron diffusion coefficient as a function of temperature for silicon.[4]



Solid solubility of phosphorous and boron in silicon as a function of temperature.[5]

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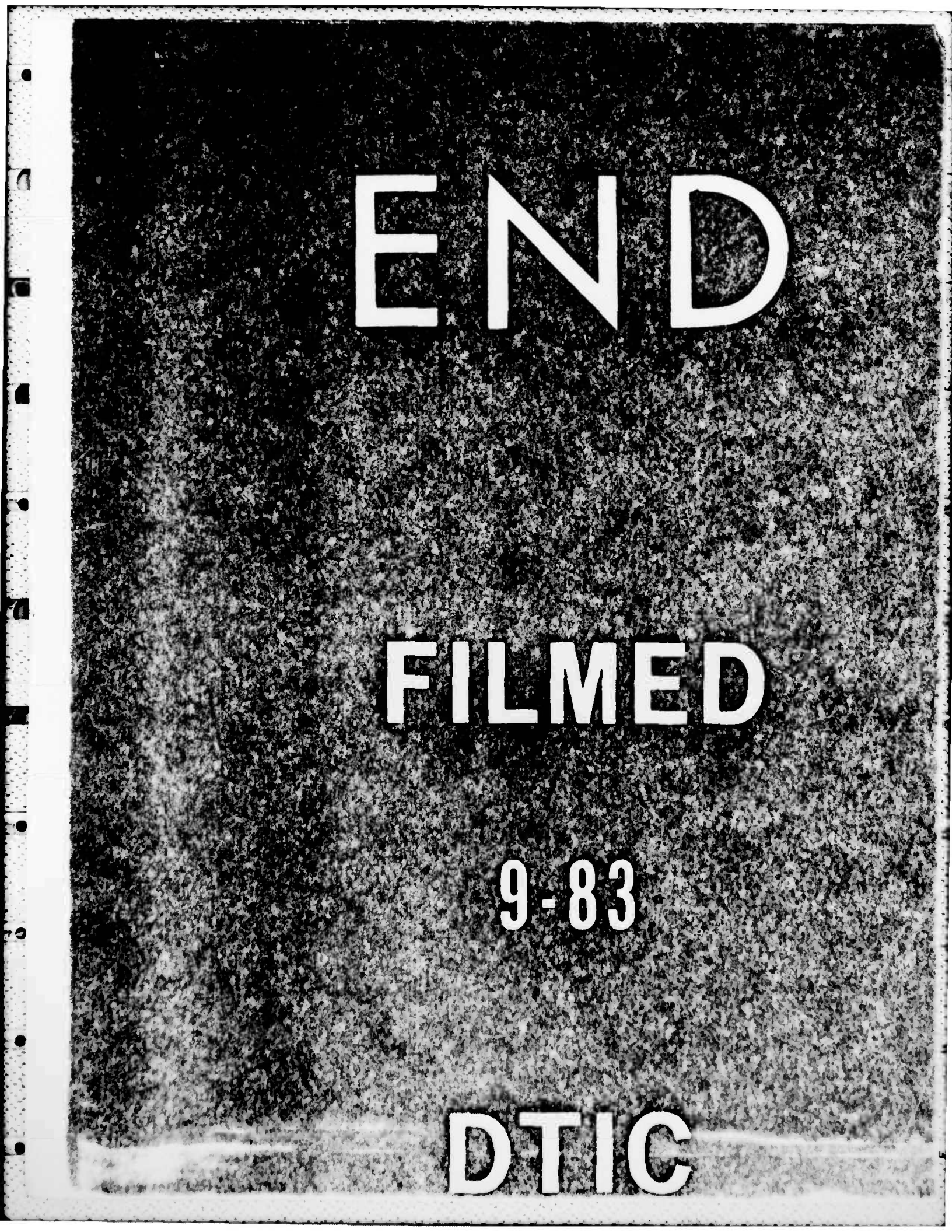
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FILMED
9-83
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Background Concentration cm-3